WIRELESS POWER MANAGEMENT CIRCUITS FOR BIOMEDICAL IMPLANTABLE SYSTEMS

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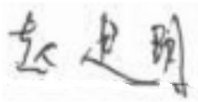
Declaration

I hereby declare that this thesis is my original work and it has been written by me in its entirety. I have duly acknowledged all the sources of information which have been used in the thesis.

This thesis has also not been submitted for any degree in any university previously.



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SUMMARY

In this thesis, a wireless power recovery system with data link for implantable systems and a new full-wave active rectifier with high power efficiency are described. The power recovery system is designed to provide supply for a high-compliance-voltage neural/muscle stimulator. It provides 3 DC outputs: 1.8 V, 3.3 V and 20 V for the stimulator with bidirectional data link. A 2-stage time division based rectifier is proposed to provide 3 DC outputs simultaneously, improving the power efficiency without introducing any impact on the forward data recovery. 1.8-V and 3.3-V supplies are provided by two low voltage regulators. The 20-V output is generated by a modified low ripple charge pump that reduces the ripple voltage by 40%. The power management system is fabricated in a 0.18-μm CMOS process with 24V HV LDMOS option, occupying a core area of around 3.5 mm^2. The power management system shows 49% peak power efficiency. The forward and backward data rates of the data telemetry are 61.5 kbps and 33.3 kbps, respectively. In addition, a power monitor circuit for closed-loop power control is integrated.

In the second part of the thesis, an active full-wave rectifier for wireless power recovery is presented. The rectifier dynamically senses the conduction time error caused by carrier voltage amplitude and frequency variation, and compensates the error by adjusting the comparator input offset through a proposed algorithm. In addition, two-comparator topology is used to generate the control signal to turn on and off one conduct transistors, respectively. In this way, conduct time is maximized and multi-conduction problem is

completely eliminated. This new rectifier is able to maintain good power efficiency in a wide carrier amplitude and frequency range. Fabricated in a 0.35-μm CMOS process, the rectifier achieves greater than 80% power efficiency with a 500 Ω load resistor from 100 kHz to 6 MHz at wide carrier amplitude with a peak efficiency of 83.4% at 2 V DC output voltage and 13.56 MHz carrier frequency. The chip occupies 0.3mm^2 core area.

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LIST OF ABBREVIATIONS

AC	Alternating Current
ASK	Amplitude Shift Keying
BMI	Brain Machine Interface
CDR	Clock Data Recovery
CMOS	Complementary Metal Oxide Semiconductor
DC	Direct Current
DC-DC	DC to DC converter
FES	Functional Electrical Stimulation
FSK	Frequency Shift Keying
HV	High Voltage
IC	Integrated Circuit
LDO	Low Dropout Regulator
LSK	Load Shift Keying
LV	Low Voltage
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NMOS	N-channel MOS
PE	Power Efficiency
PFM	Pulse Frequency Modulation
PMOS	P-channel MOS
POR	Power On Reset
PSK	Phase Shift Keying
RF	Radio Frequency
UWB	Ultra Wideband

VCO	Voltage Controlled Oscillator

CHAPTER 1

INTRODUCTION

Benefited from continuous performance improvements of integrated circuits (IC), biomedical circuits and systems have found increasing number of applications in medical therapy and personal healthcare. These bioelectronic systems provide alternative ways to the traditional theraputical techniques. The low power consumption and wireless power/data link allow the system to be implanted in human body without the need for wired connection on the body. Among these applications, brain-machine interface (BMI) and function electrical stimulation (FES) have recently drawn a lot of research interests, for the prediction that the technology advance will cure some nerve-related illness.

A typical BMI, as shown in Fig. 1.1 [1], consists of neural signal recording unit, a wireless power/data link, and a signal processing system to extract

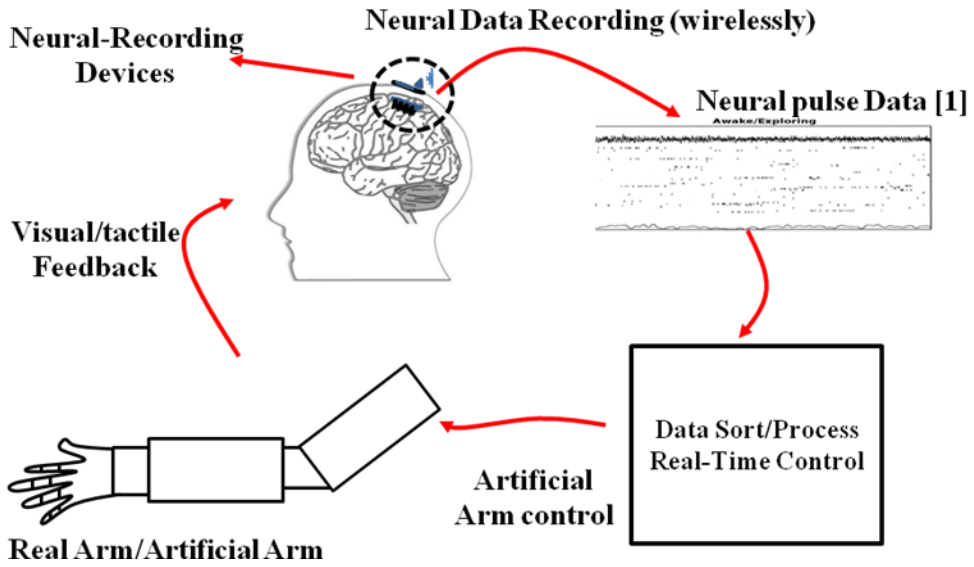


Figure 1.1. Paradigm of a BMI close loop system.

meaningful information for control of an artificial device or stimulating target nerve or muscle to recover the lost function caused by the damage in central or peripheral nerve system [2-9]. Considering non-invasive electrode scheme shows slow speed to extract meaningful signal and high sensitivity to noise interference, fully implanted invasive electrode paradigm is now treated as the most promising way to achieve aim of the BMI. To get more useful data, hundreds-channel, several years, recording paradigms are carried out. More importantly, the data are transmitted wirelessly to computer，which enables freely moving monkeys brain activity recording

FES, on the other hand, has several types of applications, including pacemaker [10,11], brain stimulation to treat neural disorders, pain [12] and Parkinson's disease and implant devices for auditory and visual function restore [13,14], peripheral neuroprostheses [15-17], as shown in Fig. 1.2.

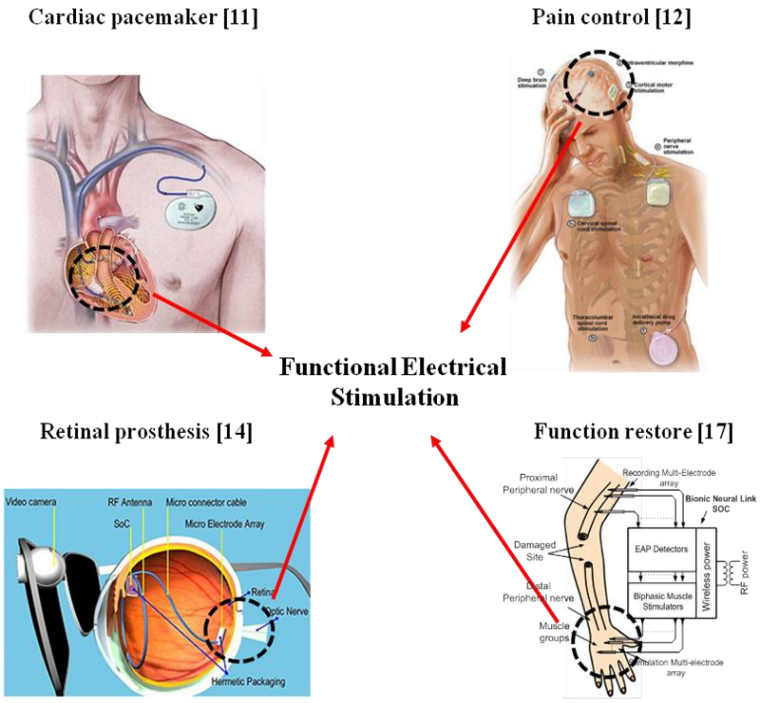


Figure 1.2. Typical applications of FES.

Among them, pacemaker, hearing aid (cochlear) and epiretinal prostheses are commercially available, whereas the others are still at research stage. As we know, pacemaker is implanted in human body, powered by battery since it consumes little power and the battery can last more than 10 years [10], and hence it is acceptable to the patients. However, implanted battery is not acceptable in other applications, such as cochlear hearing aid implant and some neuroprotheses, where relative large power consumption is required and thus the battery needs to be replaced more frequently. In such applications, wireless power is absolutely required.

1.1 Wireless Powering

Leaving wires bare from the implanted system to outside of the body is not always acceptable because it becomes less reliable when animal moves around. More importantly, the baring wound will cause infection in a long term experiment. To supply power to the internal part without skin wound and limitation on animals' free movement, wireless powering is very crucial.

Thermal power harvest circuit, vibration mechanical power harvest circuit and telemetry link power recovery circuit have all been implemented [18,19]. Recently, ultra sonic is adopted to wirelessly supply power for dust sensors [20]. Among these methods, using RF telemetry link to power internal part is the most promising way due to its relatively higher reliability and the larger quantity of power could be transferred wirelessly. Table 1.1 summarizes the possible energy harvesting methods and the power could be supplied by these methods.

Table 1.1. Comparison of the energy harvesting methods

Energy Source	Harvested Power	Power Density
Thermal power	< 1 mW	$\mu W/cm^2$
Vibration power	< 1 mW	$\mu W/cm^2$
Ultra sonic power	~ 1 mW	mW/cm^2
RF Telemetry power	1 mW – 200 mW	mW/cm^2

Nikola Tesla is recognized as the first one to figure out wireless power transferring, using RF power with resonating L-C tank, around 1891 [21,22]. RF wireless powering used for communication was introduced in 1960s [23,24]. Later, wireless power electrical devices was developed for various applications [25]. Until 1966, a patent aimed to provide implantable units with wireless power was granted [26].

Fig. 1.3 shows the diagram of a typical implantable device using RF wireless power and telemetry data link. It consists of internal (implanted) module and the external module. The power amplifier in the external system, usually a class-E amplifier, generates an AC power signal upon an L-C resonant tank. There is another L-C resonant tank in the internal part, has same

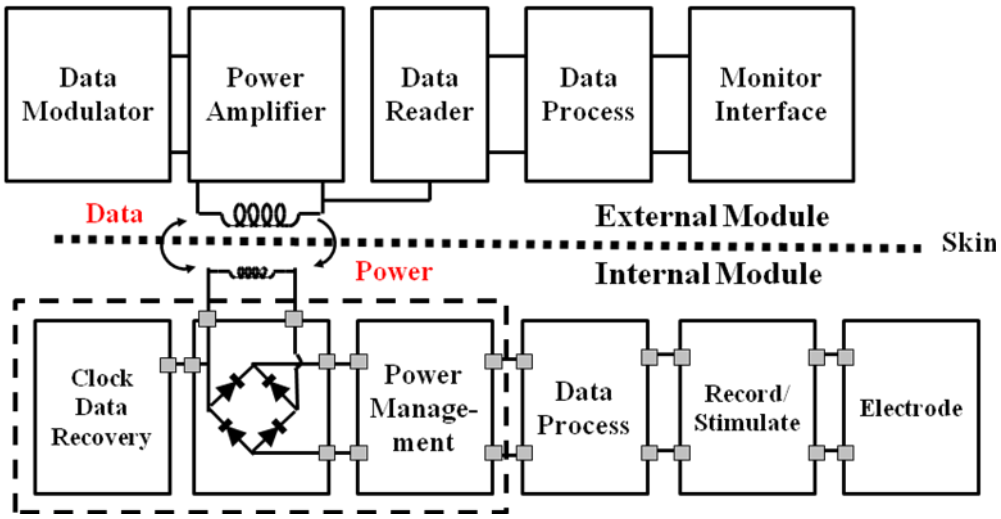


Figure 1.3. Functional blocks of an implantable system.

self-resonating frequency as the external L-C tank. The inductors in the two L-C tanks both are coils which have high mutual inductance. AC power generated by the external module oscillates with the internal resonant tank. In this way, power is transmitted wirelessly into the implantable part in animal body. This is referred to as “inductive coupling” [27-33]. In this thesis, it is near filed inductive coupling. Power carrier is 13.56 MHz and coils’ distance is 5mm.

The received AC power is transferred to DC power by a rectifier. Thus, rectifier is an indispensable block in any of this kind of system. The power received by the internal resonant tank could be influenced by many factors, such as the geometry of the coils, distance between the two coils, coil positions and self/mutual inductances. In wireless powering, the external power amplifier could be treated as voltage source with a very large equivalent internal resistance. All the parameters mentioned could change the equivalent internal resistance, thus consequently change the power received by the internal side. As a result, output of the rectifier is not stable to drive functional blocks directly. The DC power management circuit is necessary to convert the DC voltage to certain stable value to drive data processing and record/stimulate circuits.

Wireless data link is another important function for implantable devices. Generally, the forward data link (from external to internal) is used to transfer system configuration commands to the internal part, whereas the backward data link (from internal to external) is used to transfer neural activity data to the outside for processing or analysis [34-38]. The data link functional blocks are also showed in Fig. 1.3. The clock and data recovery block in the internal

Table 1.2. Comparison of the energy harvesting methods

	Carrier frequency	Forward data rate (kbps)	Backward data rate (kbps)	Output voltage (V)	Power (mW)	size	Power Efficiency (%)
[39]2005 Physiological Measurement	2 MHz	57.6	NA	±3	90	4.5 x 3 x 1.2 cm^3	25
[31]2008 JSSC	125kHz	25 – 714	Non	±2.5	NA	3.2 x 1 cm^2	NA
Proposed chip	13.56 MHz	61.5	33.3	2.8/3.3/20	25	4.3 x 1.1 cm^2	49 (receive side)

module recoveries data information and clock signal for data process. The same function block in the external module is the data reader block, which extracts data signal from L-C tank and feeds signal to data process or even monitor.

Table 1.2 summarizes three implantable modules. The first module is totally integrated with discrete components [39]. It shows the biggest PCB size. In the second module, stimulator is a custom-designed chip [31]. But the power/data link circuits are off-chip. Extra diodes, regulator and protect components are needed compared to the proposed on-chip power management circuit. In addition, the totally custom-designed chip shows better flexibility in function. It supplies more outputs, supports power monitor and provides clock to logic circuit. To reduce system size and provide adequate functions, this thesis focuses on circuits design of custom-designed chip.

1.2 Challenges in Wireless Power for Implantable Devices

Before semiconductor industry advances to sub-micron technology, the implantable stimulation system only needs one voltage to supply functional

blocks and stimulator electrodes [40,41]. However, this situation changes as the technology is developing into sub- and deep sub-micron range. Functional blocks, such as front-end and data processing circuits usually operate under a low voltage (LV) to minimize the power consumption, whereas high voltage (HV) compliance is usually required for the stimulator, in order to deliver sufficient current to the stimulation electrode [42,43]. Thus, multiple supply voltages are needed. To wirelessly supply multiple outputs and multiple voltages, several techniques have been proposed, such as using separate low-voltage and high-voltage coils, multiple low dropout regulators (LDO) or high voltage charge pump (The detailed review of these techniques will be given in Chapter 2). However, the power efficiency (PE) in such a multiple outputs wireless power recovery system still needs to be improved.

Apart from different voltage supplies, different frequency power carriers are adopted in system implementations. In such systems, a rectifier is indispensable to transfer the AC power into DC power. However, previous active rectifiers are only optimized to achieve high power efficiency at certain voltage amplitude or at certain carrier frequency. To accelerate system development and handle frequency-shift-keying (FSK) modulation on power carrier, an active rectifier with high efficiency at various carriers is required

1.3 Scope of the Research

The scope of this research is to develop high efficiency power recovery circuits for implantable systems internal modules. In the thesis, a wireless power management circuits for implantable systems internal module, such as neuroprotheses, which usually include neural signal acquisition, signal

processing, and high-voltage-compliance neural/muscular stimulator, etc. The system includes rectifier, band gap, LDOs, charge pump and other support blocks. In addition, wireless bidirectional data transmission is also included. In order to optimize PE, multiple DC output voltages are preferred. The focus of the research is to improve the PE of the power management circuits, while at the same time meeting other system performance requirements.

Moreover, a high power efficiency active rectifier is implemented. The rectifier maintain high efficiency in various cases, enabling data modulation on power carrier.

1.4 Research Contributions

In this thesis, a high efficiency wireless power recovery circuit is developed, aimed to provide the power for implantable record/stimulate systems. The research contributions are highlighted below:

1. A 2-stage 3-output rectifier is proposed. Compared to the conventional 2-stage 2-output rectifier, it can supply three different output voltages. 3 LDOs are used to stable the outputs. Working together with unbalanced L-C resonant tank, the rectifier improves the overall PE of the implantable system.
2. An improved multi-stage HV charge pump is proposed to supply high-compliance-voltage electrical stimulator. The charge pump is a 4-stage charge pump with 0.6 mA maximum load current. 2 different clocks are used in this charge pump to achieve high power efficiency and low output voltage ripple.
3. A high PE rectifier is also proposed to optimize the conduction time of the

active rectifier. In this rectifier, the effects of both circuit delay and comparator offset on the conduction time is automatically compensated through continuously tuning the offset of the specially designed comparators. Since the proposed tuning algorithm is not related to carrier frequency and voltage amplitude, the rectifier achieves high power efficiency in wide carrier frequency and input amplitude range.

1.5 Publication List

First authored:

1. **J. M. Zhao**, L. Yao, R. F. Xue, P. Li, M. K. Je and Y. P. Xu, "A wireless power management and data telemetry circuit module for high-compliance-voltage electrical stimulation applications," in *IEEE Asian Solid-State Circuits Conf. Dig. Tech. Papers*, Nov. 2013, pp. 253-256.
2. **J. M. Zhao**, L. Yao, R. F. Xue, P. Li, M. K. Je and Y. P. Xu, "An integrated wireless power management and data telemetry IC for high-compliance-voltage electrical stimulation applications," accepted by TBCAS.
3. **J. M. Zhao** and Y. P. Xu, "A high efficiency active rectifier employing dual comparators with digitally tunable offset for conduction time optimization," submitted to a journal.

Co-authored:

4. K. A. Ng, X. Liu, **J. M. Zhao**, X. C. Li, S. C. Yen, M. K. Je and Y. P. Xu, "An inductively powered CMOS multichannel bionic neural link for peripheral nerve function restoration ", in *IEEE Asian Solid-State Circuits Conf. Dig. Tech. Papers*, Nov. 2012, pp. 181-184.
5. L. Yao, **J. M. Zhao**, P. Li, X. Liu, Y. P. Xu and M. K. Je, "Implantable

stimulator for biomedical applications", in *2013 International Microwave Workshop Series on RF and Wireless Technologies for Biomedical and Healthcare Applications (IMWS-Bio 2013)*, pp. 1-3.

6. L. Yao, **J. M. Zhao**, P. Li, X. Liu, R. F. Xue, Y. P. Xu and M. K. Je, "An inductively powered implantable 20-V 1.24-mA stimulator IC with input power monitoring, active charge balancing and electrode impedance check," accepted by ASSCC 2014.

1.6 Thesis Organization

The thesis consists of five chapters. Chapter 2 describes the basic concepts of the building blocks of the power management system, including rectifier, LDO, charge pump and DC-DC converter. At the same time, literature reviews of these circuits are presented.

Chapter 3 presents a wireless power recovery system with bidirectional data link for high-compliance-voltage neural/muscle stimulator. The power recovery circuit includes a 2-stage rectifier, 2 LDOs and a high voltage charge pump to provide 3 DC outputs: 1.8 V, 3.3 V and 20 V, respectively. A 2-stage time division based rectifier is proposed to provide 3 DC outputs simultaneously. It improves the power efficiency without introducing any impact on the forward data recovery.

Chapter 4 presents an active full-wave rectifier for wireless power recovery. Digital controlled offset tuneable comparator is proposed to compensate the circuit delay and offset voltage due to carrier voltage amplitude and frequency variation. In addition, two-comparator topology is utilized to generate the control signal for rectifier switches. This new rectifier maintains high power

efficiency with a wide carriers' amplitude and frequency range.

Chapter 5 concludes the thesis and discusses the future work.

CHAPTER 2 LITERATREVIEW

Multiple outputs wireless power management system and DC-DC voltage converter circuits will be introduced and reviewed in this chapter.

2.1 Multiple outputs Wireless Power Management

There are several ways to generate multiple outputs voltages in wireless power management circuit. Using multiple LDOs on chip to supply multiple outputs voltages from one input voltage is the most straightforward way [44-46]. In these designs, an identical high voltage source is used to successfully supply all LDOs to generate multiple outputs. However, this is not an efficient way to generate multiple outputs spread over wide voltage range since the LDOs supplying the lower voltages suffer from low PE. In another work, a dual voltage scheme with two separate half wave rectifiers to simultaneously generate a positive and a negative output with same voltage amplitude for a high voltage stimulation is proposed [47,48]. However, the low voltage output is missing.

In order to supply LV and HV simultaneously, several wireless multi-voltage power modules have been reported for high-voltage-compliance stimulator. In general, they can be divided into two categories. In the first category, as shown in Fig. 2.1(a), the secondary coil supplies HV to the power management circuits [36,37]. Thus the HV output can be obtained via a HV rectifier and a LDO regulator. The LV output can be derived from either an additional coil or from LV tap in the secondary coil. In this case, the power efficiencies of HV and LV circuits cannot be simultaneously optimized since

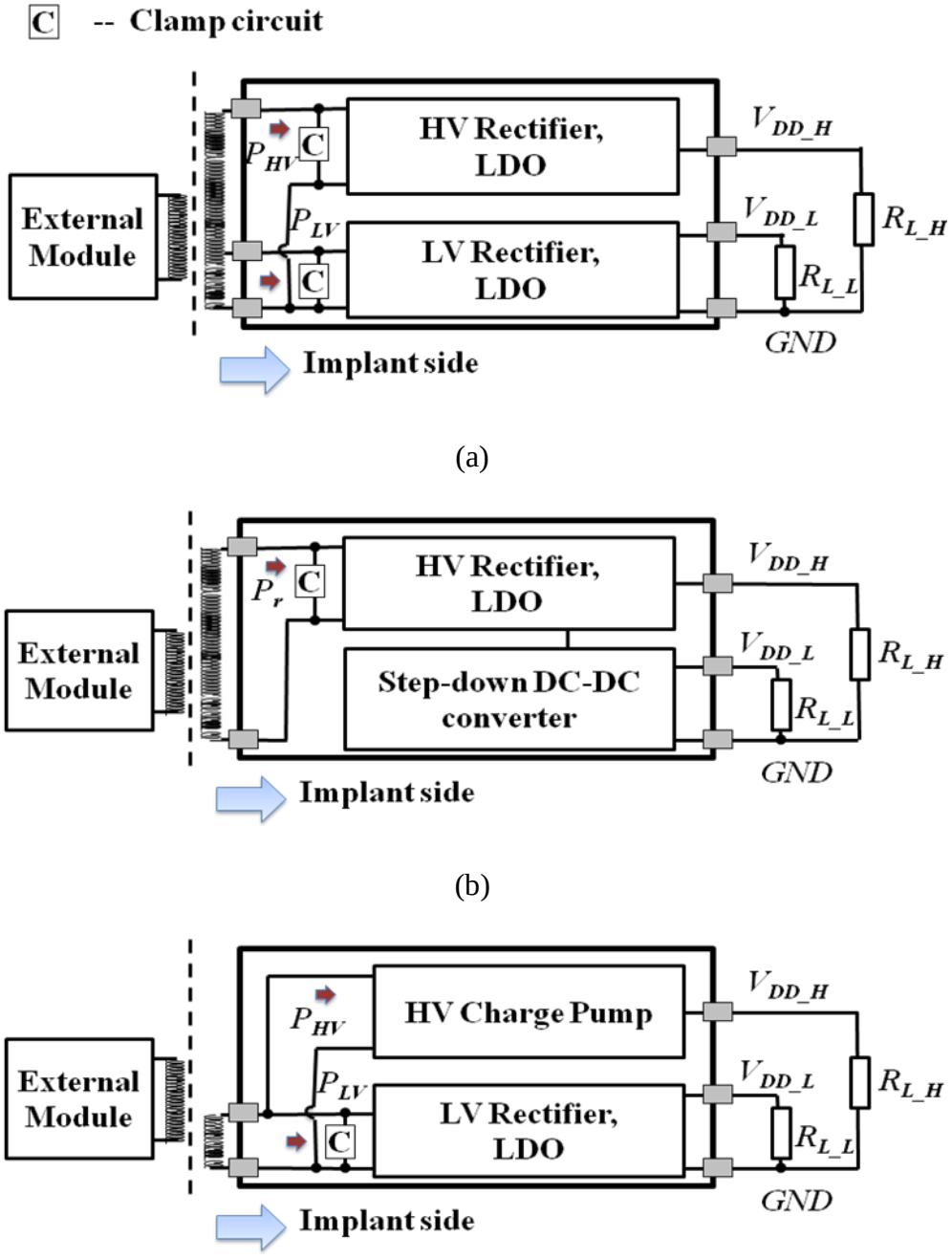


Figure 2.1. Illustration of power management system architectures to generate both high and low voltage supplies through coupling coils: (a) architecture in [36,37]. (b) Architecture in [49] and (c) architecture in [50-52].

the required amounts of power on HV and LV circuits are not proportional, but the configuration of coil is fixed after implantation. To overcome this problem a step-down charge pump can be used to supply LV output [49], as

shown in Fig. 2.1(b). HV rectifier, though simple, shows low reliability under heavy load current [49]. In the second category, the secondary coil only provides LV output. Thus, the LV output can be easily obtained through a LV rectifier and a LDO regulator, while the HV output needs a step-up DC-DC converter, as shown in Fig. 2.1(c) [50-52].

Depending on the distance of the coupling coils and the loading conditions, the voltage from the secondary coil (internal coil) may fluctuate in a wide range, and cause circuit failure. A clamp circuit is usually required to protect the power management circuit when the voltage goes excessively high. It provides a leakage path whenever the coil voltage exceeds a prescribed level. The clamp circuit consumes large energy when activated and reduces the PE significantly. To avoid this, a closed-loop power control is included to control the power in the external module and transmit just right amount of energy to internal module [53]. However, for wireless high-compliance-voltage stimulator with multi-supplies, the clamp current problem and high PE techniques haven't been well addressed yet.

2.2 Rectifier

External power amplifier transfers DC power into AC power which is transmitted wirelessly through the inductive link to internal implantable part. Rectifier converts the AC power back into DC.

In CMOS technology, MOS switches are used in place of diodes in the classic rectifier. Based on whether switches are controlled, rectifier can be categorized into passive and active rectifier. Fig. 2.2(a) and 2.2(b) show the concept of passive [54-57] and active rectifiers, respectively, in which

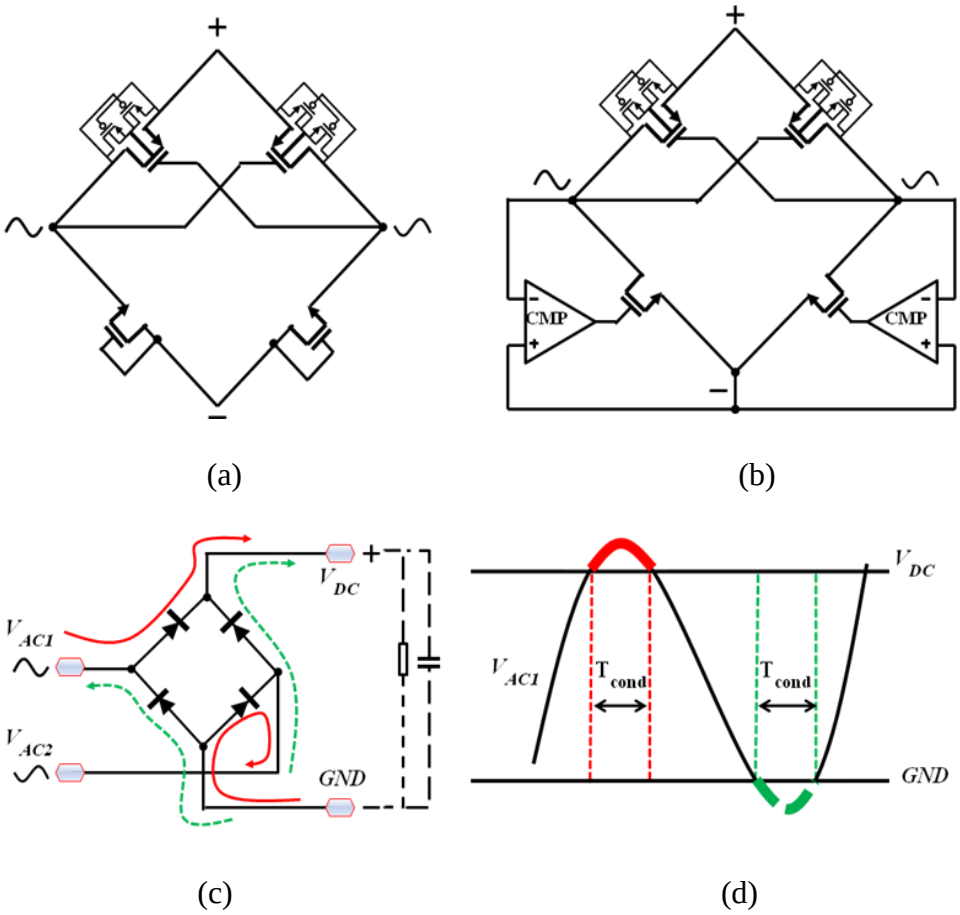
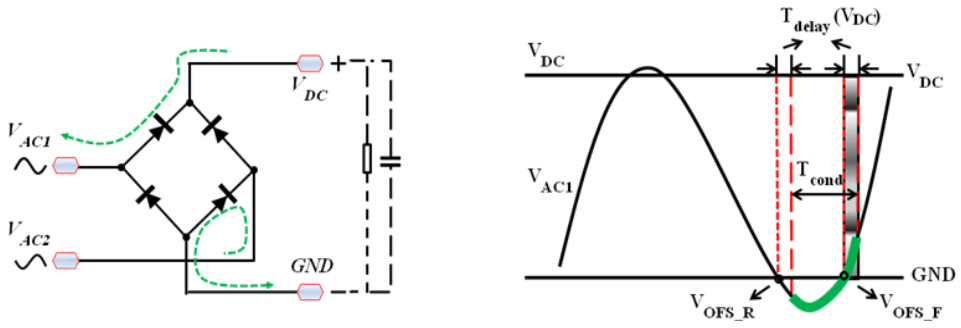


Figure 2.2. Diagram of a rectifier schematic and the wave forms. (a) Diode-connected passive MOS rectifier. (b) Switch based active MOS rectifier. (c) diagram of a full-wave rectifier and current flow paths. (d) The rectifier's conduct period, T_{cond}.

MOSFETs are used to implement the diode in Fig. 2.2(c). To reduce V_{th} voltage drop in passive rectifier, active rectifier are proposed to achieve high PE [58-60]. In the active rectifier, comparators are used to turn on and off of the bottom two "diodes", which reduces the forward voltage drop to $2V_{DS}$, much less than the diode forward voltage drop of 0.7V. In an ideal rectifier, the correct current flows and conduction periods are shown in Fig. 2.2(d).

For active rectifier, in order to achieve high PE, comparator needs to generate just right drive signals to maximize the possible conduct time of the rectifier without causing reverse current. However, the circuit delay and



(a) (b)

Figure 2.3. (a) Reverse current flow path. (b) Conduct period with the same VOFS_R and VOFS_F.

comparator offset may lead to incorrect conduction of the transistors [61,62], and reverse current, as shown in Fig. 2.3(a) and Fig. 2.3(b). V_{OFS_R} and V_{OFS_F} are input offset voltages of turn on and turn off signal that conduct transistors needed. T_{dealy} is the delay from comparator output to real drive signal of conduct transistors and it's a function of V_{DC}. During the time marked by shaded box, reverse current flows, which can severely deteriorates PE. To mitigate this problem, unbalanced-biased comparator has been proposed to prevent reverse current at a carrier frequency of 1.5 MHz [61]. To achieve high PE at higher carrier frequency, say, up to 13.56 MHz, comparator with dynamic offset adjustment [63-67] and cross-coupled latch comparator [62] are proposed to speed up the comparator. Dynamic offset adjusting comparator uses local positive feedback loop to set different on and off offset voltages (as shown in Fig. 2.4(a)) and fast turn-off signal. But this technique may cause multi-conduction of the conduct transistor due to its local positive feedback in the comparator [68-70]. Cross-coupled latch comparator technique adds another assisted comparator to speed up the main comparator. Apart from modifying the comparator design, adjusting signal delay to avoid the reverse

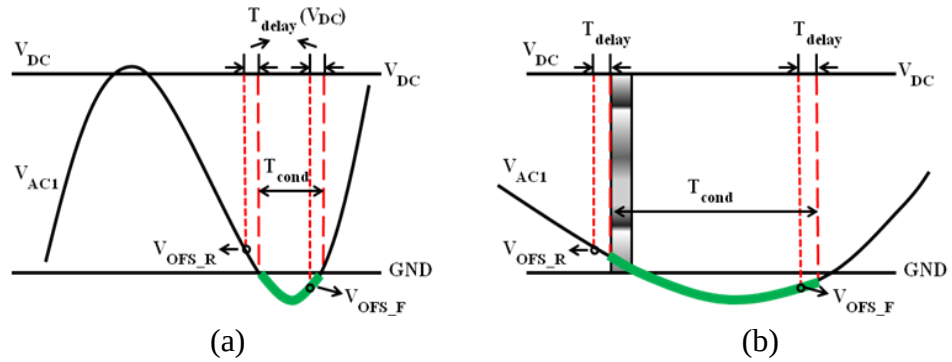
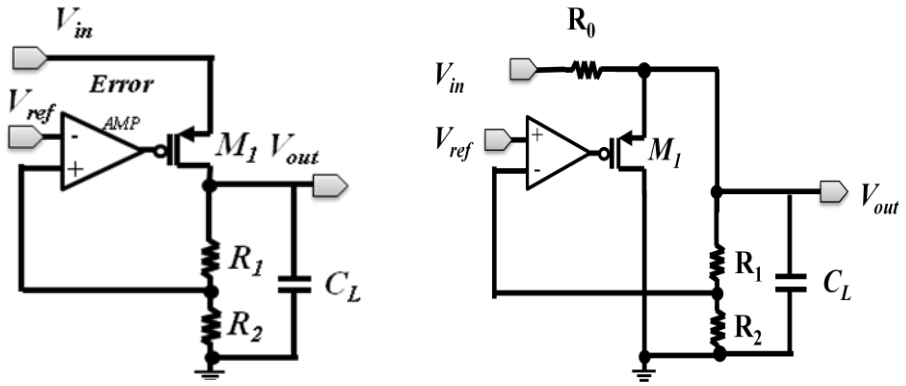


Figure 2.4. Working conditions of a rectifier with the same input offset voltage comparator with (a) just right frequency carrier and with (b) lower frequency carrier.

current is also proposed [36]. However, reverse current cannot be totally avoided in a wide input voltage amplitude range by above mentioned techniques, since the circuit delay varies with carrier amplitudes and is very difficult to be accurately controlled. To deal with the wide input amplitude problem, dynamic biasing comparator technique [68] is proposed to compensate the varying circuit delay using carefully designed bias current for the comparator. However, multi-conduction is not absolutely eliminated since local positive feedback is still used.

On the other hand, for possible frequency-shift-keying (FSK) data modulation on power carrier [71], a rectifier whose PE is optimized for wide carrier frequency range and different input amplitudes is very desirable. For example, the frequency of V_{AC1} in Fig. 2.4(a) is just four times of the frequency of V_{AC1} in Fig. 2.4(b) and comparator offset voltages are same. But PE of the rectifier in Fig. 2.4(b) is much lower due to reverse current. All above mentioned rectifiers only optimize the PE for at a fixed carrier frequency.



(a) (b)

Figure 2.5. Schematic of (a) series connected type LDO. (b) parallel connected type LDO.

2.3 Low Dropout Regulator

LDO regulator is the most widely used voltage converter to supply constant voltage for its simplicity and good transient response performance.

LDO regulator includes a power transistor (M_1), a resistor voltage divider (R_1 and R_2), an error amplifier (Error AMP) and a voltage reference, as shown in Fig. 2.5. LDO can be categorized into two topologies, serial-connected (Fig. 2.5(a)) and parallel-connected topologies (Fig. 2.5(b)). The resistor divider samples the output voltage and feedback it to the error amplifier which compares the feedback voltage with a reference voltage. The extra power exceeds necessary is dissipated on the power transistor as drop voltage in serial-connected LDO or leakage current in parallel-connected LDO.

Recently, output-capacitor-less LDO has been reported. It has the advantages of less pin count, smaller PCB area, and no parasitical effects of equivalent inductance/resistance from wire-bond [72]. Another research direction in LDO is the digital LDO, in which the analog feedback loop is substituted by a digital controller. Digital LDO can operate under a very low

supply voltage since the core control circuit is digital circuit [73-75]. For wireless powered systems, it is very crucial to have high PRSS to reject the noise from the input. In [76], an output-capacitor-less LDO achieves the PSRR of -20 dB in a very wide range from 1 kHz to 11 GHz. With a ~100 mV output ripple rectifier, this design could satisfy most of the implantable systems' requirement.

The PE of the LDO is limited by the ratio of V_{out} and V_{in}. When V_{in} is much higher than V_{out}, a LDO's PE is low and it deteriorates the PE of the entire power management circuit. In multiple outputs wireless power management system, as far as the PE is concerned, it is not desirable to supply different output voltages by just using several LDOs.

2.4 Switched inductor based converter

Switched inductor based power converter (normally referred as DC-DC) shows the highest PE in all voltage converters, generally. It consists of an inductor (L), several conduct power transistors (M_1 – M_4) and feedback control unit, as shown in Fig. 2.6. The conduct transistors are connected to the two ports of the inductor and turn on/off in certain sequence. By carefully

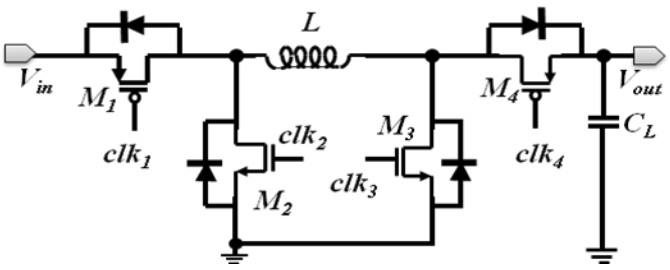


Figure 2.6. Diagram of a switched inductor based voltage converter.

designing the conduct transistors' driving clock sequence, the switched inductor converter can achieve buck, boost and buck/boost voltage conversion.

Recently, the research related to the switched inductor power converter mainly focuses on control method and single input with multiple outputs [77 - 84]. For high voltage DC-DC, the designers used synchronous rectification methodology, current estimate and totally digital circuit to control the boost converter with voltage conversion ratio larger than 20 [85].

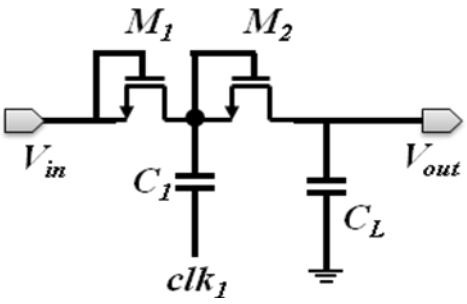
Switched inductor based converter is rarely used in wireless power management. The reason could be because the inductor in converter could interfere power transmission between the coupling coils, as well as the data link, and generate too much electromagnetic field in animal body.

2.5 Charge pump

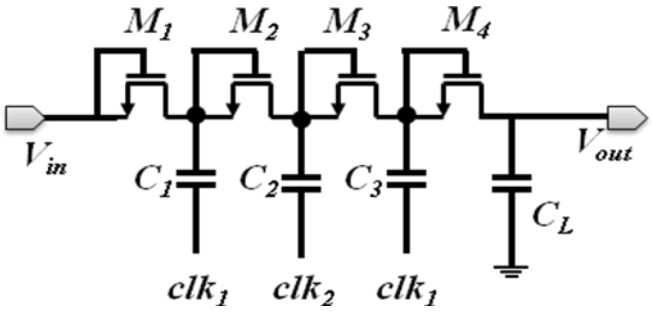
Charge pump is another type of voltage converter. Charged capacitor is utilized to pump up/down V_{in} to perform voltage conversion.

Dickson charge pump is the most original and widely used topology in designs. Fig. 2.7 shows the diagrams of a basic (a), Dickson (b) [86] and a cross coupled [87] charge pump (c), respectively. The charge pump includes the flying/load capacitors and the power transistors. The flying capacitors (C_1 – C_3) store the electrical energy from the input source in one clock phase and release the energy to the output in another phase. The load capacitor (C_L) stabilizes the output during the period when the flying capacitors is disconnected from the output. The power transistors (M_1 – M_4) are located at the two ports of the flying transistors to control the flying capacitors.

In 1992, the charge pump controlled by MOS switches was introduced in



(a)



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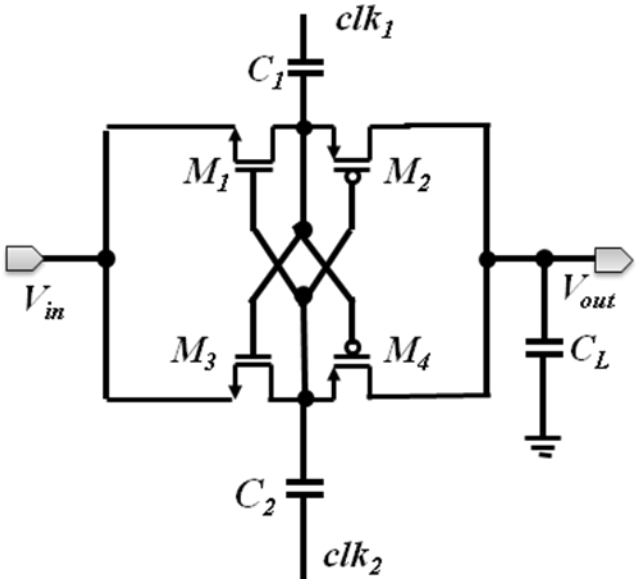


(c)

Figure 2.7. Diagram of (a) Basic topology charge pump (voltage doubler). (b) Dickson topology charge pump. (c) Cross coupled topology charge pump.

[88]. The cross coupled charge pump was reported to eliminate voltage drop

on diode connected power transistors, V_{th}, in Dickson topology [87]. Bi-directional power flow charge pump [89] and programmable multi-mode charge pump [90] were also proposed. Reconfigurable charge pump has since become popular since charge pump PE is enhanced when V_{in} significantly fluctuate.

To improve PE, dynamic dead-time control to reduce the shoot-through current, and the shared-charge recycling technique are developed to enhance PE of charge pump [91,92]. In HV compliance stimulator, to boost the input voltage of 5V to around 20 V, HV multi-stage charge pump is required. Suppose there are two charge pumps, a LV charge pump converts 1.5V to 6 V and another HV charge pump converts 5V to 20 V. Let the other parameters are same, high voltage design consumes 11 times more power than low voltage on parasitic capacitors. When the charge pump has several stages, the whole power efficiency is product of every stage efficiency, which is also harmful for power efficiency. However, no effective technique has been introduced to achieve high PE in HV multi-stage charge pump implementation. Table 2.1 shows electrical characteristics summary of previous work to supply very high voltage with low input voltage.

The output of the charge pump usually contains ripple, resulted in from the switching of the capacitors. Some ripple voltage reduction techniques have been reported [98-100]. Controlling the voltage drop of power transistor not only regulates output voltage but also reduces output ripple voltage [98]. However, it shows lower PE in light load than that in pulse frequency modulation (PFM) technique since its clock frequency is fixed. The interleaving regulation with multi-phase clocks [99] reduces the ripple, but

Table 2.1. Comparison of the charge pumps with high voltage conversion ratio

Paper	PE (%)	Input (V)	Output (V)	Stage	Fly. Cap.	Max. Cur.	Frequency	Technique
[93]	91(SOI)	3.3	27	9	18	40 uA	4 MHz	0.35 µ m SOI CMOS
[94]	NA	2.5	28.08	12	12	NA	1 MHz	0.25 µ m CMOS
[95]	NA	3	>15	3	4	2 mA	0.5 MHz	HV CMOS
[96]	NA	2	6.5/ -6	2/2	4/4	300 uA	100 MHz	0.8 µ m CMOS
[97]	NA	3.3	9/ -9	2/3	10	160 uA	36 MHz	0.18 µ m CMOS

needs a dual power stage, which increases the circuit complexity and number of capacitors. Dynamically changing the size of the charge pump driver together with PFM in [100] can reduce the ripple, but results in higher clock frequency and degrades the PE.

2.6 Wireless Data Link

Wireless data link is another important function for implantable bio-systems. Low power consumption, high reliability, wide bandwidth, small size and light weight are the key points that need to be considered. Below some data modulation schemes used for bio-medical systems will be reviewed.

2.6.1 Amplitude Shift Keying (ASK)

ASK is widely used in biomedical systems for its design simplicity [101,102]. In ASK modulation, the amplitude of the carrier is modulated by ASK modulator and the demodulator recovers the serial data by comparing the amplitudes of the carrier envelops. The disadvantage of ASK modulation is its sensitivity to the carrier amplitude. In practice, body movement or other factors may influence the carrier amplitude, which leads to malfunction of the

ASK data link.

2.6.2 Load Shift Keying (LSK)

LSK modulation is almost the same with ASK. The only difference is the way the amplitude is modulated. LSK refers to the backward data modulation scheme through suddenly change the internal load to modulating the carrier [64,103]. Besides of the same drawback as ASK, LSK doesn't work when the two power transferring coils are loosely coupled. In this situation, the load shift at the internal side can no longer induce voltage fluctuation on the external coil.

2.6.3 Frequency Shift Keying (FSK)

Compared to ASK, FSK is more reliable since the carrier frequency won't be influenced easily as carrier amplitude. The carrier frequency will shift from one frequency to the other during FSK modulation [104,105]. The disadvantage of the FSK modulation is that the wireless power transfer efficiency is reduced due to resonator tank's low Q at two different frequencies.

2.6.4 Phase Shift Keying (PSK)

PSK modulates the carrier by shifting carrier's initial phases. The drawback of PSK is the complex demodulator circuit to correctly recover the phase information, and its power consumption is usually higher than ASK and FSK [37].

2.6.5 Ultra Wide Bandwidth (UWB)

UWB is recently used in biomedical systems for its high data rata and low

power consumption. A serial of non-continuous pulses are generated to denote "1" or "0". The challenged of USB circuit design is its antenna miniaturization and high PE pulse generator. In [106], a 2 MHz data link is implemented by using optical data link. Its work principle is similar to UWB modulation. This method is effective in Retinal Prosthetic devices but may not be suitable for the internal system that is deeply implanted in body.

Each modulation scheme has its advantages and disadvantages. Table 2.2 summarizes their key performance parameters. The transmission distances are not applicable for the references. In these examples, UWB shows the best performance compared to the other modulation method. A practical way to design a good wireless data link is to choose the right modulation according to the application. For example, the forward and backward data links definitely

Table 2.2. Different modulation schemes in biomedical applications

Year	Power	Carrier Freq	Data rate	Modulation	Power/bit	Applications
2000 [101]	NA	1-10 MHz	25-250 kbps	ASK	NA	Retinal Prosthetic
2008 [102]	0.3 mW	2 MHz	1 Mbps	ASK	300pJ/b	Biomedical app
2008 [103]	NA	500 kHz	16 kbps	LSK	NA	Biomedical app
2011 [64]	NA	13.56 MHz	500 kbps	LSK	NA	Inductively link
2004 [104]	~0.4 mW	5/10 MHz	2.5 Mbps	FSK	160pJ/b	Biomedical app
2013 [105]	NA	3.2/3.8 GHz	48 Mbps	FSK	NA	Neural Sensing
2010 [37]	NA	22 MHz	2 Mbps	PSK	NA	Retinal Prosthetic
2009 [36]	1.6 mW	163 MHz	90 Mbps	UWB	18pJ/b	Neural Recording
2012 [106]	0.3 mW	NA	2 Mbps	Photodiode	150pJ/b	Retinal Prosthetic

have different requirements. Combining two or more modulations together is a way to achieve good performance. In this thesis, ASK and LSK are adopted for simple circuit implementation.

CHAPTER 3 AN INTEGRATED WIRELESS POWER MANAGEMENT AND DATA TELEMETRY IC FOR HIGH-COMPLIANCE-VOLTAGE ELECTRICAL STIMULATION APPLICATIONS

In this chapter, a power management chip with data telemetry for neural/muscle stimulation is described. Table 3,1 summarizes the key parameters of a muscle/nerve stimulator Three voltage supplies are required, 1.8V, 3.3V and 20V with maximum load current of 200μA, 200μA and 1mA, respectively. Recovery time means the 20V output can drop to certain value when stimulating with large current, but it should rise to normal value in certain time after one stimulating.

A LV 2-stage rectifier is proposed to generate three DC outputs for a 1.8V LDO, 3.3V LDO and a 20-V charge pump to enhance power efficiency

Table 3.1. Stimulation required specifications

	Parameter	Value	Unit	Remarks
Power/data link	clock frequency	13.56	MHz	ASK
	modulation	30	kbps	ASK forward, LSK backword
	20V load current	1	mA	
	3.3V load current	200	μA	
	1.8V load current	200	μA	
	Standby ripple	0.2	V	
	Recovery time	0.5	ms	

without compromising the performance of the data link. The two LV supplies are directly obtained through the two LDOs, respectively, and the HV supply is generated by the step-up 20-V charge pump. A low ripple voltage step-up HV charge pump based on the PFM technique is proposed to reduce the output ripple and achieves high power efficiency [107]. A wireless bidirectional data telemetry is also implemented on chip. With a power monitor circuit, the power system is able to transfer power status data from the internal module backward to the external module to support the wireless closed-loop control of the power transmitted from the external module to the internal module.

The rest of the chapter is organized as follows. Section 3.1 describes the system architecture, as well as the 2-stage rectifier and the low ripple step-up charge pump. Section 3.2, section is circuit implementations. Section 3.3 presents the measurement results and discussion.

3.1 System Description

Fig. 3.1 shows the functional block diagram of the power/data recovery IC and its targeted application is to high-compliance-voltage neural/muscular stimulator. Three output voltages are 1.8 V for digital control circuit, 3.3 V for analog circuit and 20 V for HV-compliance output stage of the stimulator. A wireless bidirectional data link is also included on chip.

A 13.56 MHz power carrier is chosen for both power and data telemetry. A LV L-C resonator tank on the secondary side receives the transmitted power. A 2-stage rectifier generates three LV DC voltage sources. A capacitor, C_{DC} is inserted between the L-C tank and RF1- for DC voltage shifting. The 1st stage rectifier generates the lowest voltage, which is regulated by a LDO to obtain

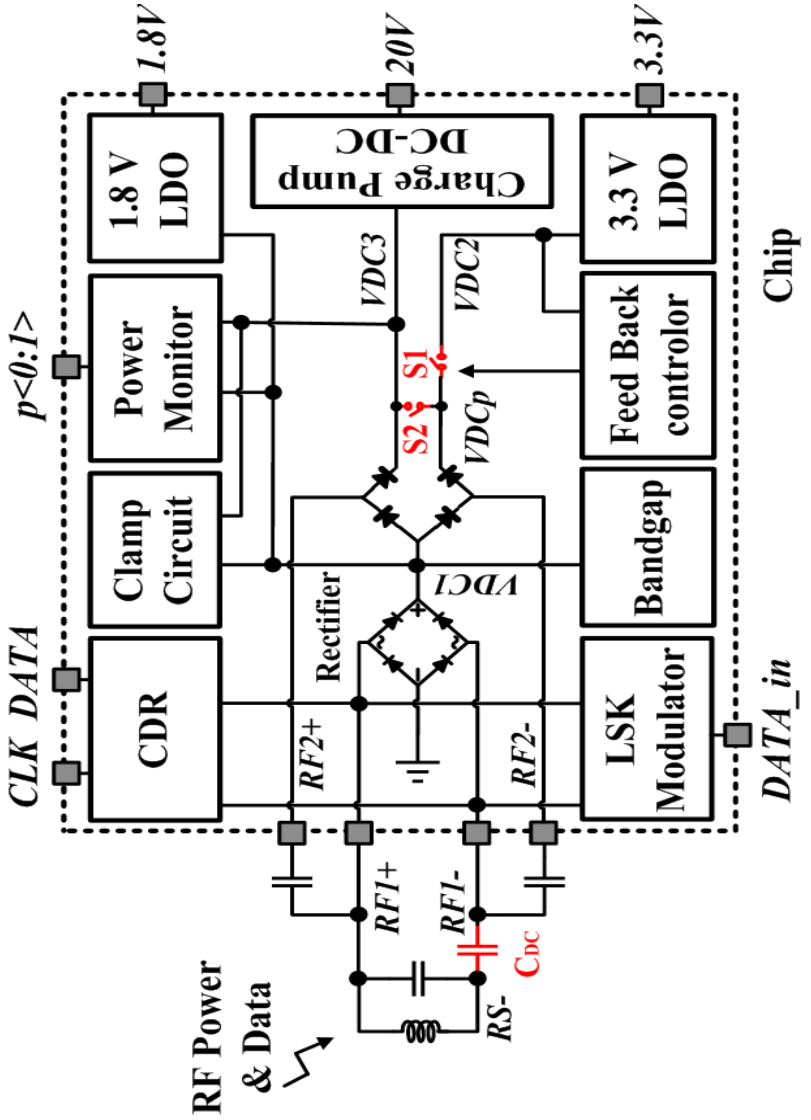


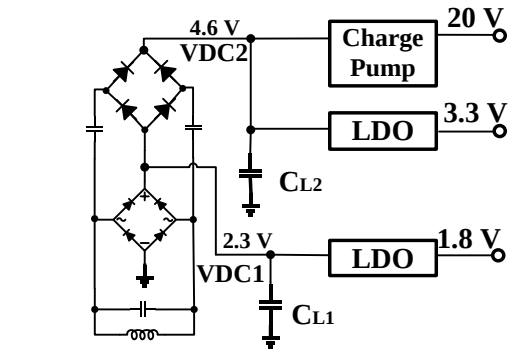
Figure 3.1. Functional block diagram of the power/data recovery system.

1.8 V. The 2nd rectifier stage can be configured into either a full-wave rectifier or two half-wave rectifiers through two switches and generates two slightly different voltages: 3.6 and 4.6 V for the 3.3-V LDO and the charge pump in a time-division fashion. A feedback control circuit controls the time-division or the working mode of the 2nd rectifier stage. The detailed operation principle of the proposed 2-stage rectifier will be described in section 3.1.1.

For wireless data telemetry, CDR circuit is connected to RF1+ and RF1- for clock and data recovery. The clock signal is directly recovered from the 13.56 MHz carrier, RF1+. The ASK forward data signal is extracted by an envelope detector. A LSK modulator for backward data telemetry takes feedback data, such as that from simulator, and modulates the loading on RF1+ and RF1- [108,109]. A data reader at the external module can recover the backward data.

3.1.1 The proposed 2-stage rectifier

In this design, the minimum input voltage for 1.8-V and 3.3-V LDOs are 2.1 V and 3.6 V, respectively. For the step-up charge pump, a highest possible input voltage is preferred to reduce the number of charge pump stages. However, the gate-source break down voltage of the HV transistor is 6 V for the chosen CMOS process. Thus, the desired input voltage range for the charge pump is 4.2 ~5 V after leaving a safe margin for HV transistors in the charge pump. Based on aforementioned considerations, a 2-stage rectifier could be used to generate all three output voltages, as shown in Fig. 3.2(a). The 1st stage provides the supply for 1.8-V LDO and it should be higher than 2.1 V whereas the 2nd stage should be higher than 4.2 V for the charge pump. The 3.3 V can be derived from 4.2 V output with a LDO. However, by doing so, it would incur extra power consumption in the LDO, which reduces its power efficiency. In this work, a 2-stage rectifier is proposed to supply three different voltages, e.g. 2.3 V, 3.6 V and 4.6 V, where 3.6 and 4.6 V, in a time-division manner. In such an arrangement, the 3.3-V LDO is able to maintain



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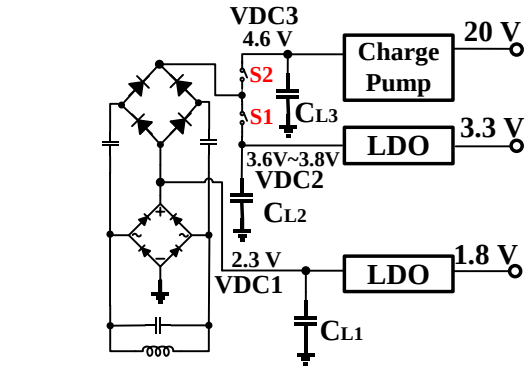

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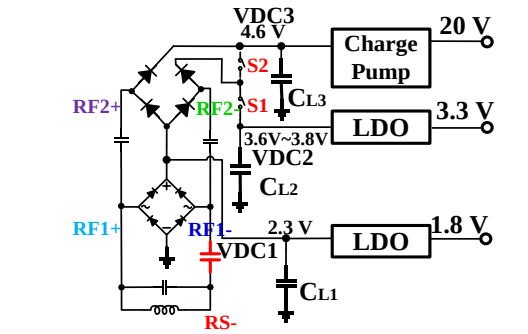

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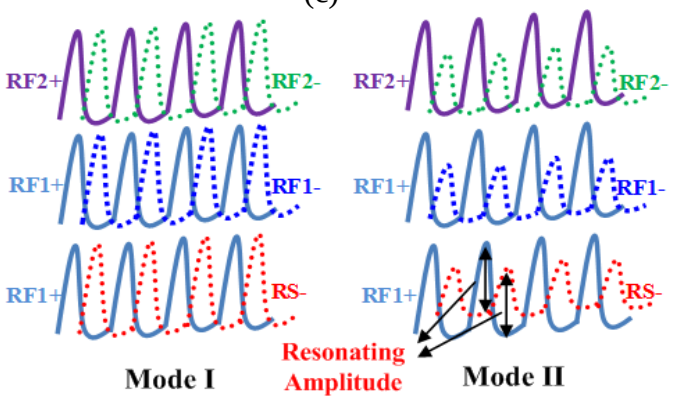


(d)

Figure 3.2. (a) Conventional 2-stage rectifier. (b) A 2-stage 3-outputs rectifier based on time division technique. (c) The proposed 2-stage 3-outputs rectifier and (d) waveforms of the proposed rectifier.

good power efficiency.

Fig. 3.2(b) shows a possible rectifier implementation based on the time-division, in which the 2nd stage rectifier supplies two outputs through switches S1 and S2. One problem with such an arrangement is that the ASK/LSK data will be corrupted by the resonating amplitude change caused by the switching between *VDC2* and *VDC3*. Another drawback is that when the second stage switches between *VDC2* and *VDC3*, it causes the 1st stage rectifier output to jump between *VDC2/2* and *VDC3/2*. Fig. 3.2(c) shows the proposed 2-stage rectifier that can overcome the above mentioned two problems. In the proposed 2-stage rectifier, a DC shifting capacitor C_{DC} is inserted between the resonator tank and the 1st stage rectifier to make the L-C tank resonating normally. The 2nd stage is divided into two half-wave rectifiers to supply two different voltages, simultaneously. The rectifier works in 2 modes. When *VDC2* is larger than 3.8 V, the rectifier switched to mode I (S1 is open and S2 is closed). The 2nd stage rectifier now works as a normal full wave rectifier to supply *VDC3*, charge C_{L3}. When *VDC2* is lower than 3.6 V, it switches to mode II (S1 is closed and S2 is open). The 2nd stage rectifier works as two half-wave rectifiers to supply *VDC2* and *VDC3*, respectively. Thus, *VDC2* is maintained between 3.6 V and 3.8 V, the rest of the energy is stored on the load capacitors at *VDC1* and *VDC3*. Fig. 3.2(d) shows the waveforms in both mode I and II for the proposed 2-stage rectifier. The rectifier is same as the conventional 2-stage rectifier in mode I. In mode II, the AC amplitudes of *RF1+* and *RS-* are different. But the resonating amplitude, |(*RF1+*) – (*RS-*)| is constant, referred to as "unbalance resonating", that is, *RF1+* and *RF1-* have different peak voltages, but the same bottom voltage. The same applies to *RF2+* and *RF2-*. Furthermore, unlike the rectifier in Fig. 3.2(b), ASK signal

on the 13.56 MHz power carrier is not affected in the proposed 2-stage rectifier.

3.1.2 Low ripple voltage multi-stage charge pump

The step-up charge pump is chosen as it can be fully integrated on-chip and has better transient response than the inductor based DC-DC converters. Since the stimulator is not always firing, charge pump is in light load most of the time. PFM is well suited for such applications [110]. The power loss of the charge pump can be expressed as

$$P_{loss} = f_{clk} C_{par} V_{sw}^2 + N_{sta} R_{on} I_{load}^2 \quad (1)$$

where f_{clk} is the switching clock frequency, C_{par} is the capacitance of the parasitical capacitor, V_{sw} is the voltage swing of the switches, N_{sta} is the stage number, R_{on} is the switch on-resistance and I_{load} is the load current. For a multi-stage HV charge pump, lowering the clock frequency can enhance the charge pump power efficiency. However, low clock frequency results in large ripple at the output.

Some ripple voltage reduction techniques have been reported [98-100]. In this work, we propose a simple ripple reduction scheme where the last transistor in the output stage of the charge pump is controlled by a high frequency clock. This scheme can reduce the ripple voltage without significant impact on the power efficiency of the charge pump. Fig. 3.3(a) shows the conventional PFM control scheme. Charge pump transfers large amount of power in every clock phase at a low clock frequency for high power efficiency, resulting in a large ripple. Fig. 3.3(b) shows the proposed low ripple control method. A higher frequency clock is used only for the last transistor in the

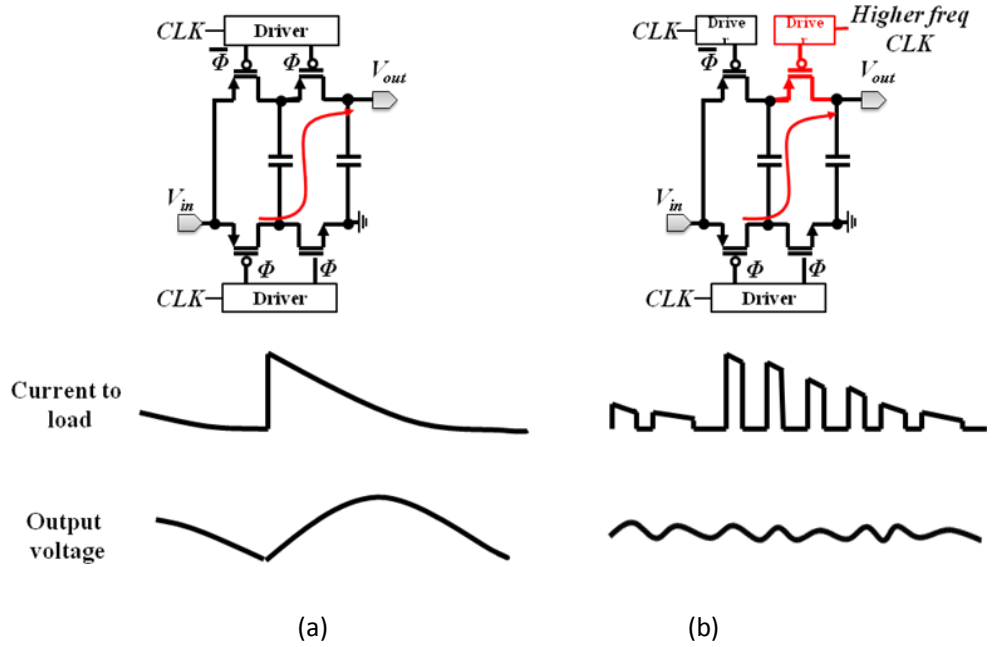


Figure 3.3. Illustration of the proposed charge pump ripple reduction method: (a) conventional single clock and (b) the proposed 2-clocks work principle.

output stage, M_{out}. This allows the charge to be delivered more accurately and smooth the voltage ripple at the output. The implementation of the high-frequency clock is based on the current re-use, which will be explained in section 3.2.2. It works well with the PFM control scheme and will be discussed in the next section.

3.2 Circuit Implementation

3.2.1 2-stage 3-outputs rectifier

The RF power received through the L-C tank is rectified by the 2-stage rectifier with dynamic body bias, as shown in Fig. 3.4. In the 1st stage of the rectifier, M_{p1} and R_{p1} provide bias voltages to reduce the forward conduction voltage V_{ds} of M_{r1} and thus improve the power efficiency [111]. The resultant increase of reverse current and quiescent power consumption on M_{p1} and R_{p1} (2.5 MΩ) can be limited to a small amount by carefully selecting design parameters.

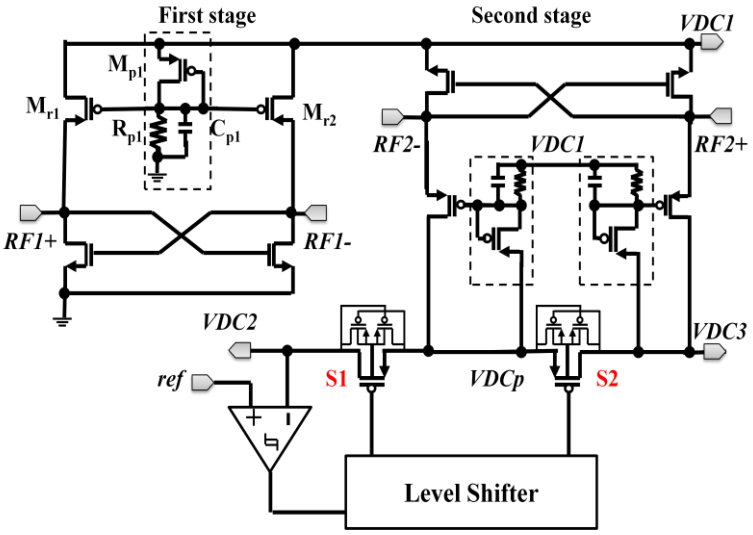
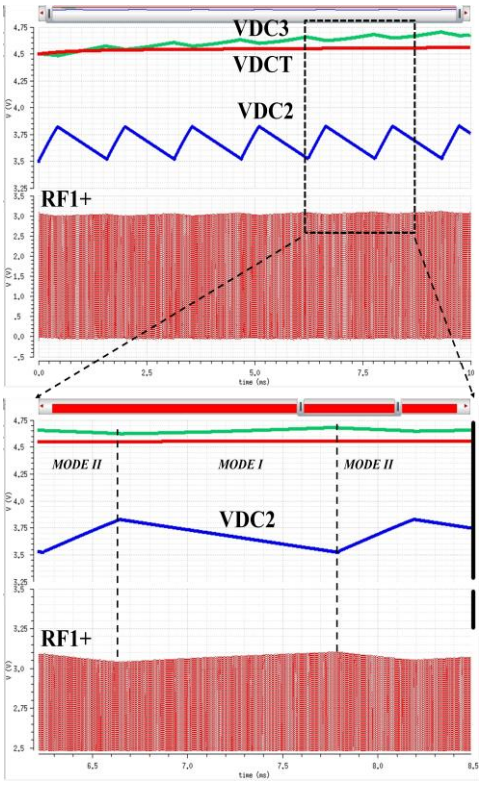


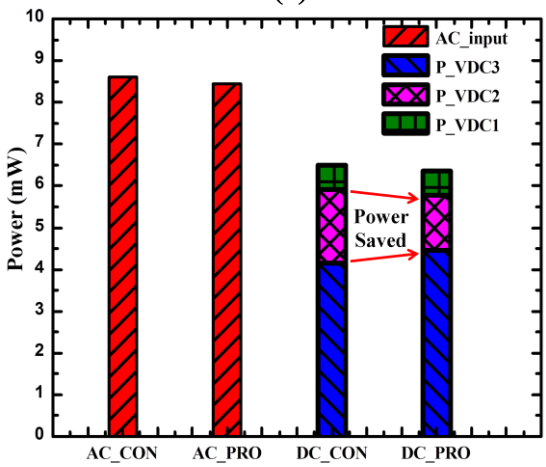
Figure 3.4. Schematic of the 2-stage rectifier.

The designed range of *VDC1* is 2.1-2.5 V. The same bias circuit is implemented for the 2nd stage rectifier which is divided into two independent half-wave rectifiers. S1 and S2 are two PMOS switches to connect *VDCp* to either *VDC2* or *VDC3*. They are controlled by a hysteresis comparator and a level shifter which directly drives S1 and S2. Cross-coupled PMOS pairs are used to supply higher voltage to bulk of S1 and S2 to eliminate latch-up. The range of *VDC2* is 3.6-3.8 V while the range of *VDC3* is 4.2-5 V. S1 is closed and S2 is opened when *VDC2* is discharged to 3.6 V. After *VDC2* reaches 3.8 V, S2 is close and S1 is open, the two half-wave rectifiers join together to charge *VDC3*.

Fig. 3.5 shows the simulation results of the proposed rectifier, compared with a conventional one. The 1.8-V LDO and 3.3-V LDO both have 360 µA current load. *VDC3* is connected to an 800µA current source to mimic the charge pump current consumption driving 100 µA load. The conventional rectifier in Fig. 3.2(a) with the same load conditions is used for comparison. Fig. 3.5(a) shows the simulated input and output waveforms of the proposed



(a)



(b)

Figure 3.5. Simulation results of the proposed rectifier: (a) waveforms of *VDC2*/ *VDC3* in the proposed rectifier and Waveform of *VDCT* in the conventional rectifier. (b) power comparison of the proposed rectifier with the conventional one. *AC_CON* and *AC_PRO* are power wirelessly received by conventional and the proposed rectifier, respectively. *VDC3*, *VDC2* and *VDC1* are the DC power consumed on *VDC3*, *VDC2* and *VDC1* (for the conventional rectifier the 2nd stage DC power is VDC3+VDC2).

rectifier in both operation modes, where *VDCT* is the output of conventional 2-stage rectifier. *VDC3* gradually becoming higher than *VDCT* indicates that

under the same current loads, more power is stored on capacitor, C_{L3}, which is desirable, while *VDC2* is maintained between 3.5V and 3.8V. Fig. 3.5(b) shows that there is a power saving in the *VDC2* 3.3-V LDO in the proposed rectifier, which results in 6.3% improvement in power efficiency (*DC_CON*/*AC_CON*) of the whole system. In the zoomed-in view of *RF1+* in Fig.3.5(a), the transition between mode I and mode II causes very tiny change on *RF1+*. This means that the mode change does not have any impact on ASK signal.

3.2.2 Low Ripple HV Charge Pump and LDOs

A step-up charge pump is used to boost the output of the rectifier (*VDC3*) to 20 V. Fig. 3.6 shows the complete block diagram of the PFM controlled HV step-up charge pump. It consists of core circuit of charge pump, a current reuse V-to-F converter, clock generation circuit and LV/HV drivers.

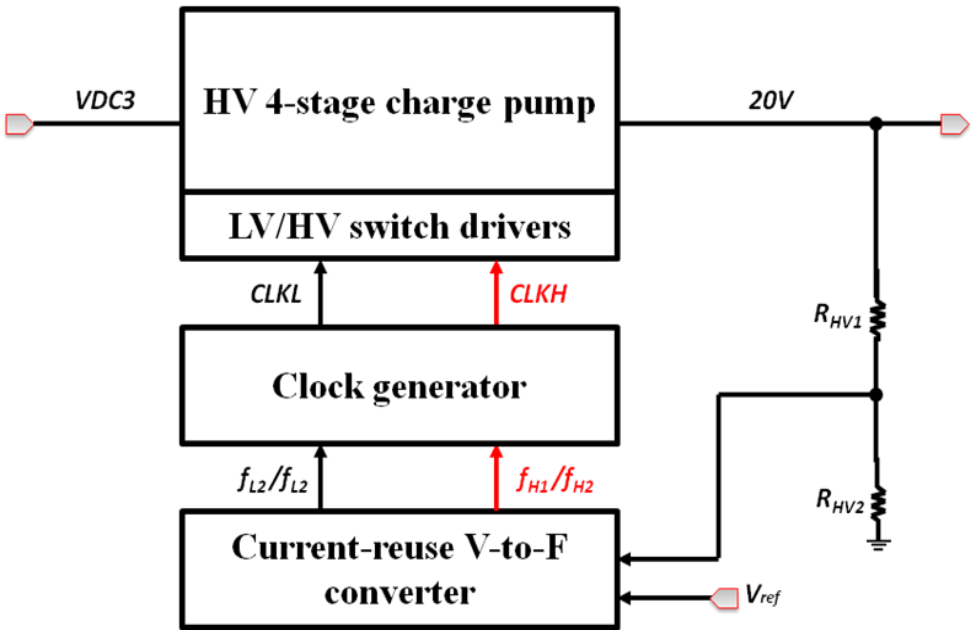


Figure 3.6. Block diagram of the HV charge pump.

The core circuit is a 4-stage charge pump, as shown in Fig. 3.7. The 24-V LDMOS process supplies 24V asymmetric NMOS and PMOS. The transistors' V_{DS} and V_{GD} can sustain 24 V, but transistors' V_{GS} break down voltage is only 6 V. Except of the LV driver in broken line box in figure 3.7, all the other transistors are all 24V LDMOS. In this charge pump all transistors V_{DS} is equal or smaller than Vin (<5V) and transistors gate voltage is connected to drain or source in different clock phases. In this way, transistors are protected from break down.

The 4th stage of the charge pump employs cross-coupled structure to reduce the voltage ripple at the 20V output. In charge mode, ϕ is "0", C_{F1}, C_{F2}, C_{F3} and C_{F4a} are charged by their preceding stages. C_{F4b} discharges to C_L at the output. Voltages at S1, S2 and S3 nodes decrease and the output is maintained by V_{S3} + VC_{F4b}. In discharge mode, ϕ is "1", C_{F1}, C_{F2}, C_{F3} and C_{F4a} are discharged and C_{F4b} is charged by S3. Voltage at S1, S2 and VS3 increase and

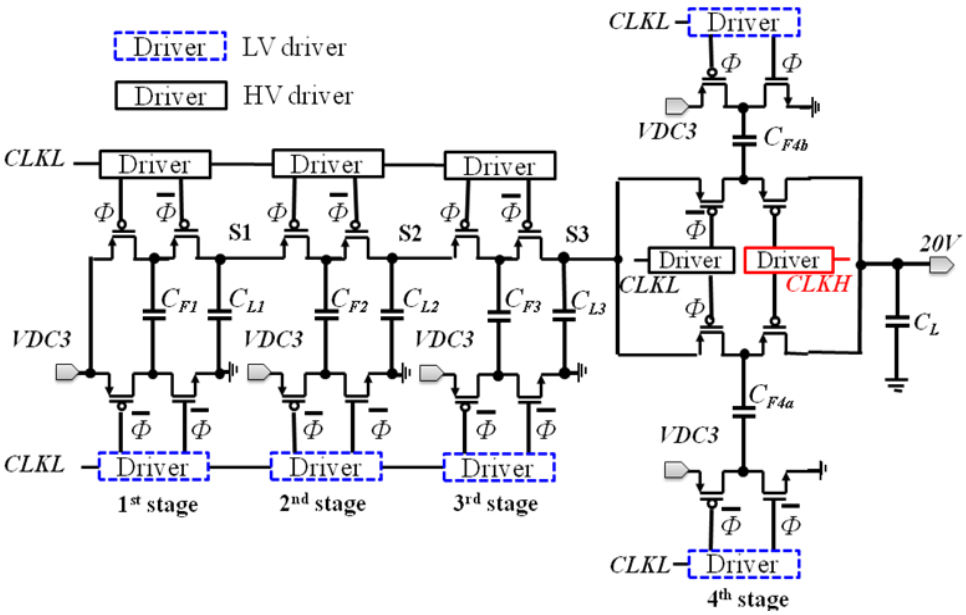
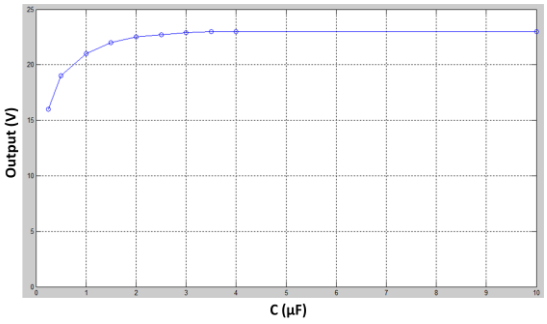


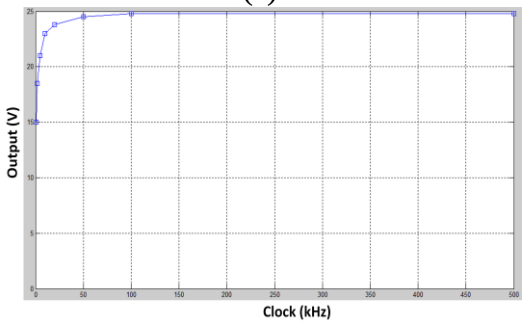
Figure 3.7. Core circuit of the 20 V charge pump.

output voltage is supplied by V_{S3} + VC_{F4a}. V_{S3} is the voltage of S3. VC_{F4a} and VC_{F4b} are the voltages on capacitors C_{F4a} and C_{F4b}, respectively.

Fig. 3.8 shows charge pump output vs. flying capacitance and output vs. clock frequency. The charge pump has been optimized to 1 μF flying capacitor and 5 kHz frequency. Too high clock frequency needs very large area for the switches. The reasonable transistor size leads to tens of kilo hertz clock frequency. For even higher power efficiency, the several kilo hertz clock frequency is chosen and the flying/loading capacitors are calculated by $C=I_{load}/\Delta V f$ (ΔV=200mV).



(a)



(b)

Figure 3.8. (a) Charge pump output vs. Flying capacitance and (b) charge pump output vs. clock frequency.

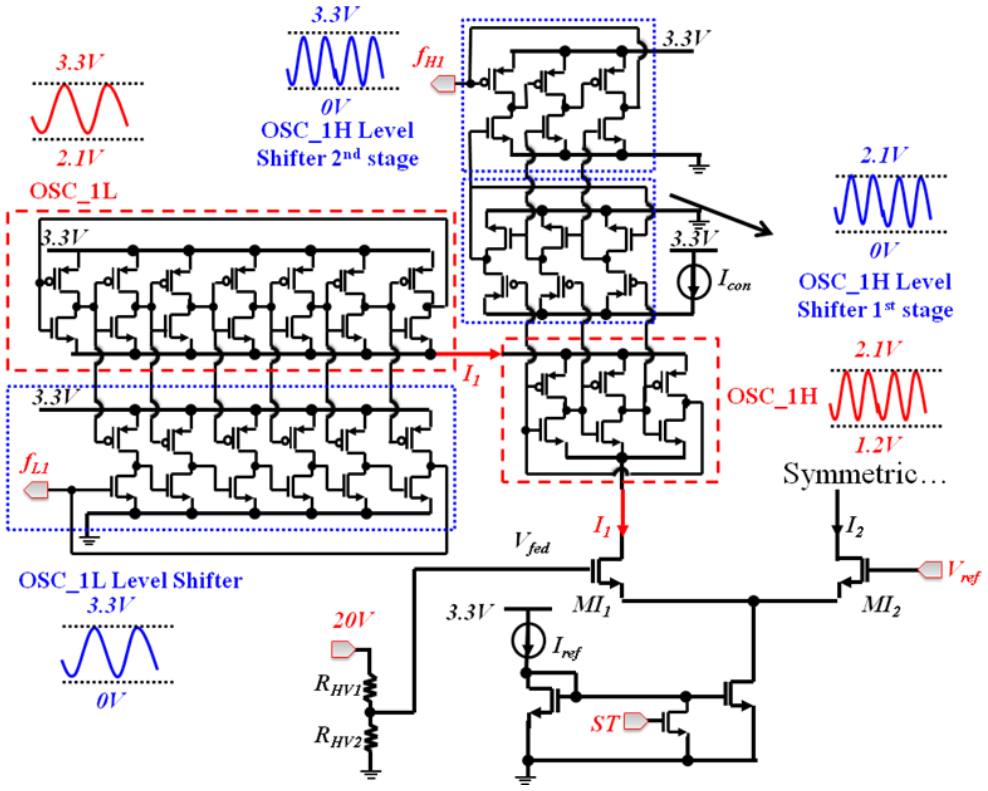


Figure 3.9. Schematic of the current -reuse V-to-F converter.

The PFM control circuit includes a voltage sensing circuit consisting R_{HV1} and R_{HV2}, the proposed current re-use V-to-F converter, clock generation circuit and LV/HV drivers. The current reuse V-to-F converter performs error comparison and converts the voltage error to frequency through a differential VCO pair. Fig. 3.9 shows the detailed schematic of the V-to-F converter. It is modified from [112] with current re-use technique. A differential pair (M_{I1} and M_{I2}) drives four ring oscillators with two on each side. Since both sides are symmetrical, only one side is shown in Fig. 3.9. OSC_1L is a 7-stage ring oscillator whereas OSC_1H is a 3-stage ring oscillator. Two ring oscillators are connected in serial and re-use the same current. This not only saves the power, but also makes the two oscillators track each other. OSC_1L and OSC_1H outputs swing from 2.1 to 3.3 V and 1.2 to 2.1 V, respectively. The

oscillating signals need to be shifted to full logic scale of 0 to 3.3 V, thus level shifters are needed. OSC_1L is directly shifted to the full logic scale, OSC_1H is shifted to 0-to-2.1V first and then 0-to-3.3V through two level shifters, as shown in Fig. 3.9. The level shifter chain must be carefully designed to prevent it from self-oscillating. The startup of the V-to-F converter is controlled by signal ST which is enabled after 1.8-V LDO and 3.3-V LDO successfully start up.

The clock generation circuit monitors the frequencies of these four oscillators (f_{L1}, f_{H1}, f_{L2} and f_{H2}) and generates two clock signals (*CLKL* and *CLKH*) to control the 20 V charge pump through LV/HV drivers. *CLKL* determines the entire charge pump clock phase shifting and *CLKH* controls the switches in the output stage and reduces the output ripple. The frequency of *CLKL* is designed to be low (< 10 kHz) to avoid significant switching power consumption on parasitic capacitance. The frequency of CLKH is set to be around 6×*CLKL*, above which the ripple reduction shows little further improvement. The LV/HV switch drivers are designed to have low current dissipation and sharp clock edge. Protect circuit is also included in the high voltage charge pump [113].

Fig. 3.10 shows the simulation results of the charge pump with/without the high-frequency clock, *CLKH*. When *CLKH* is activated, the ripple voltage at 20-V output is reduced by more than one half compared with that uses only low frequency clock *CLKL*. In simulation, input voltage is 4.6 V and load current is 500 μA.

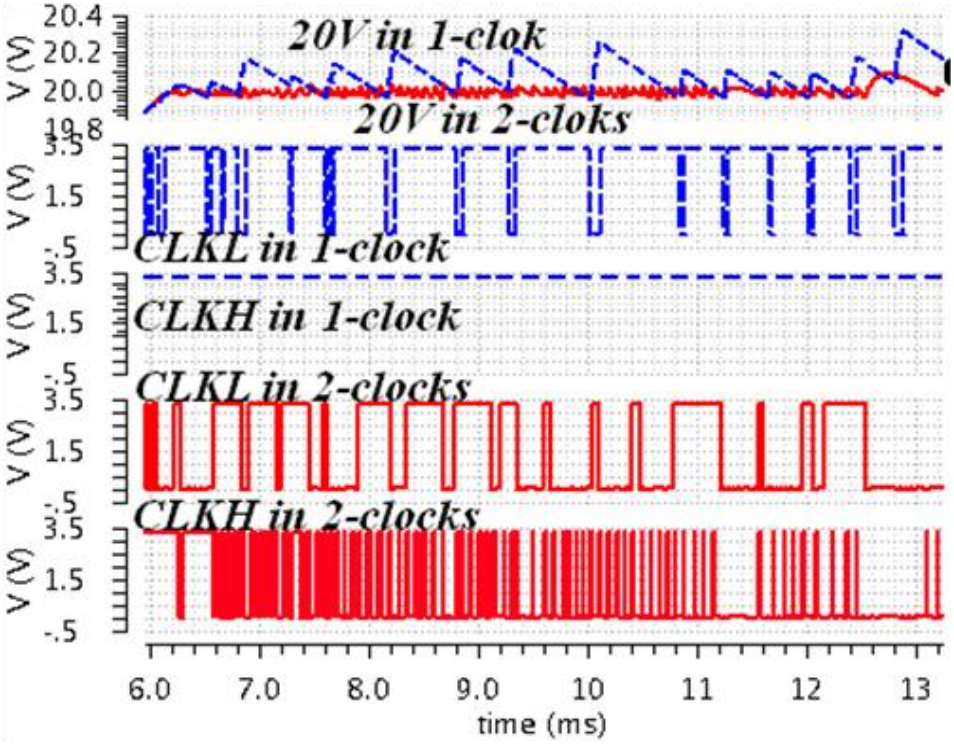


Figure 3.10. Simulation results of the charge pump 2-clocks ripple reduction..

Two LDOs are powered by *VDC1* and *VDC2*, and generate 1.8 and 3.3 V, respectively. The schematic of LDOs is shown in Fig. 3.11. The same structure is utilized for both LDOs.

3.2.3 Clocks and Data Recovery and Power Monitor

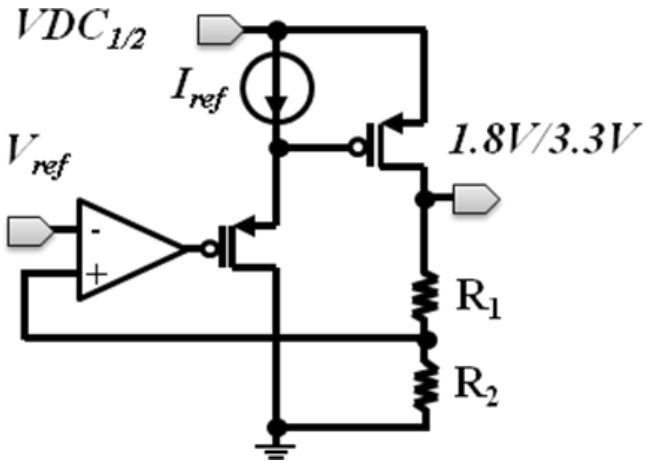
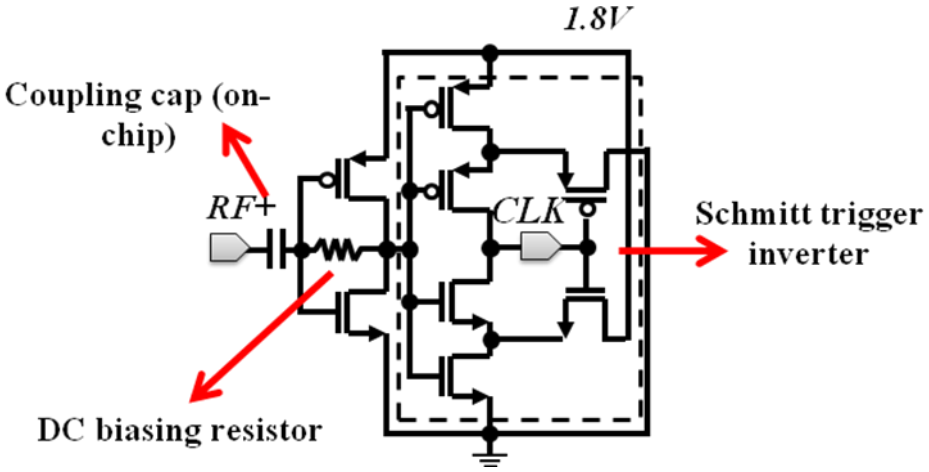
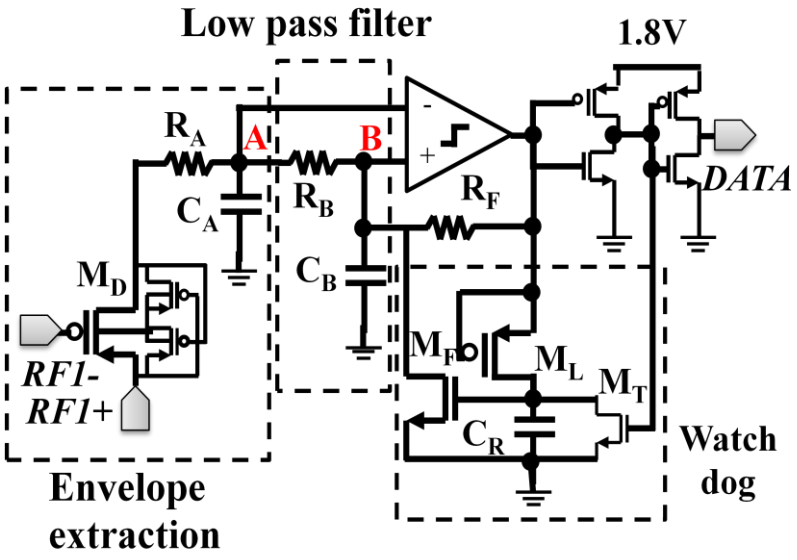


Figure 3.11. Schematic of the LDOs



(a)



(b)

Figure 3.12.Schematic of CDR: (a) clock recovery circuit and (b) ASK data recovery circuit.

The clock recovery circuit is based on a smith trigger inverter, as shown in Fig. 3.12(a) [114]. *RF1+* is fed into the circuit through a capacitor. The data recovery circuit is shown in Fig. 3.12(b). The forward ASK modulated RF carrier signals, *RF1+* and *RF1-*, are connected to a PMOS transistor, M_D, acting as a detector. A passive low pass filter consisting of R_A and C_A is used to extract the data envelope from the detector output. Another passive low

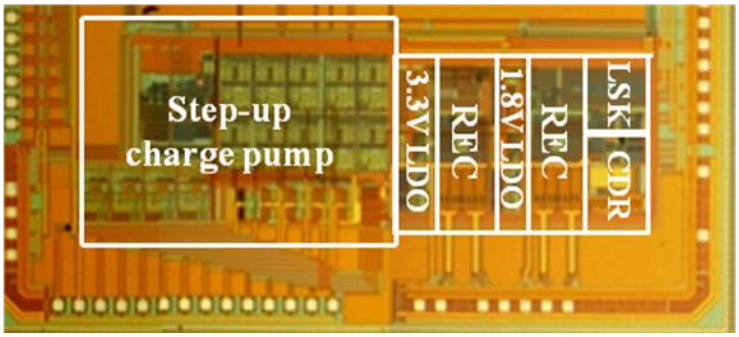
pass filter with lower cut-off frequency is used to extract the average voltage of the envelope. The data is recovered through a comparator and a buffer by comparing the envelope at A with average voltage of the envelope at B. A feedback resistor R_F is used to introduce a small hysteresis voltage (+30mV) between A and B to increase the robustness of the data recovery circuit. The correct standby state of DATA should be '0'. However, there is a risk to form a false latch through R_F where the voltage between A and B is -30mV, causing DATA to be '1' in standby state. To prevent the false standby state, a watch-dog circuit is implemented to avoid the false latch. When the comparator works in normal condition, the output of the comparator won't stay in high condition for a long time, the voltage on C_R is 0 for M_T discharge. If the comparator locks in wrong state, the output will always be high. The voltage on C_R will be charged slowly by M_L. When the voltage exceeds V_{thn}, NMOS M_F will turn on and the comparator positive input voltage becomes smaller. In this way, the comparator comes back into normal condition. Then the output goes to low, C_R is discharged again, turns off M_F. The watch dog circuit is shut down.

The LSK modulator is a set of switches, which short RF1+ and RF1- with different resistors thus change the loading of the L-C tank. The modulation depth can be adjusted based on the trade-off between the power requirement and the demodulation of the data reader at the external side.

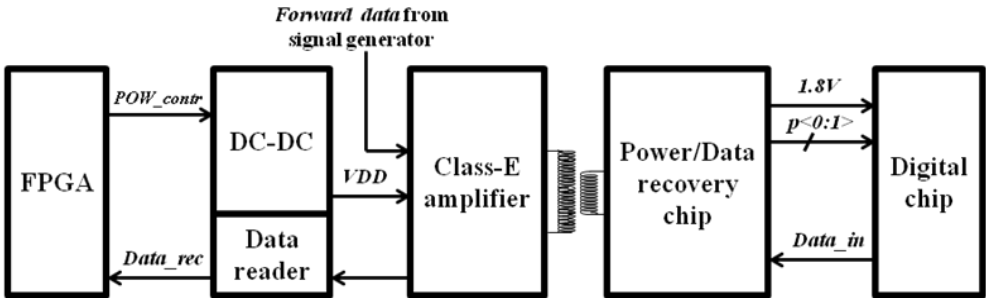
Power monitor circuit consists of two comparators powered by 1.8 V. It monitors the voltages of *VDC1* and *VDC3*. A 2-bit output digital signal *p<0:1>* indicates three states: "00" for under-powered or start up, "01" for proper-powered and "11" for over-powered.

3.3 Measurement and Discussion

The wireless power management and bidirectional data telemetry circuit was fabricated in a 0.18-μm CMOS technology with 24V LDMOS option. Fig. 3.13(a) shows the microphotograph of the chip. Fig. 3.13(b) shows the measurement setup for the functional verification of the wireless power management. RF1+ and RS- are connected to the secondary coil. The external primary coil is driven by a class-E power amplifier whose supply voltage is controlled by FPGA. The space between the two coils is 5 mm and the detailed information can be found in table 3.2. The load currents for 1.8-V LDO, 3.3-V LDO and charge pump are set to be 360 μA, 360 μA and 100μA, respectively. All the subsequent measurements are done under the same loads,



(a)



(b)

Figure 3.13 (a) Die photo of the power/data recovery module and (b) measurement setup.

Table 3.2. System parameters

System	
Technology	0.18 μm CMOS
Area	~ 3.5 mm²
Coupling Coils	
External coil	9.6 μH
Internal coil	2.1 μH
Coils' distance	5 mm
Wireless Power Management	
Carrier frequency	13.56 MHz
Outputs	1.8V/3.3V/20V
Rectifier PE	77 %
LDOs $I_{standby}$	30 μA*
Charge pump PE	82 %
Total PE	49%
Bidirectional Data Telemetry (forward/backward)	
Mode	ASK/LSK
Data rate	61.5k/33.3k bps
Power	17 μW/1.2 μW*

*Simulation results

unless specified otherwise.

The measured performance of the power management part and circuit parameters are summarized in Table 3.2. Power efficiency (PE) of individual block is measured using different optimal loads. The overall PE is calculated with three 100μA/300μA/500μA current loads connected with 1.8V/3.3V/20V outputs, respectively. Table 3.3 is the performance comparison with the

Table 3.3. Comparison with previous works

	[42]ISSCC 2013	[49]TBCAS 2011	[51]TBCAS 2011	This work
Process	32 V 0.18μm CMOS	20 V HV CMOS	0.35μm CMOS	24 V 0.18μm CMOS
Area (mm²)	NA	4/9	1.5 x 1.6	~ 3.5
Frequency (MHz)	2	13.56	0.256	13.56
Power Supply (V)	±12 V, ± 1.8 V	50 V/20 V **	5.8 V, 2 V, 1.4 V	20 V, 3.3 V, 1.8 V
Power Efficiency (%)	81(HV rectifier)	90(rectifier, sim)	NA	49
DC-DC type	HV/LV rectifier + LDO	HV rectifier + step-down charge pump	LV rectifier + step-up charge pump + LDOs	2-stage LV rectifier + step-up charge pump + LDOs
Forward Data modulation	DPSK	OOK	PSK	ASK
Data Rate (kbps)	2 Mbps @ 20 MHz carrier*	300	~ 60	61.5
Backward data rate	Non	Non	Non	33.3 kbps (LSK)
Closed-loop power control	Non	Non	Non	Yes

* The forward data link uses another antenna.
** The step-down DC-DC is not integrated in the same chip.

similar power management circuits reported previously for biomedical implantable systems.

The total PE denotes this module's peak power recovery efficiency and is calculated with three 100μA/300μA/500μA current loads connected with 1.8V/3.3V/20V outputs, respectively. The used equation is

$$\mathrm{PE}_{\mathrm{overall}} = \frac{\text{effective DC output power}}{\text{AC input power}}$$

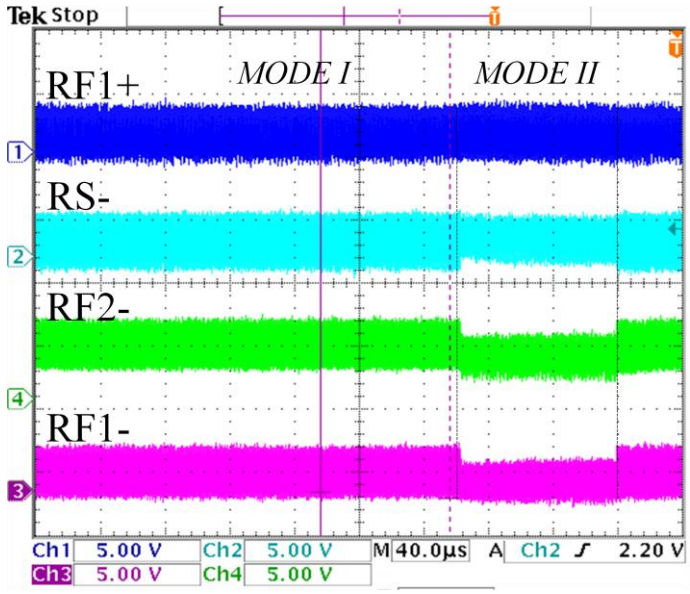
$$= \mathrm{PE}_{\mathrm{rec}} \cdot \left(\frac{\text{LDO current}}{\text{total current}} \cdot \mathrm{PE}_{\mathrm{LDO}} + \frac{\text{charge pump current}}{\text{total current}} \cdot \mathrm{PE}_{\mathrm{CP}}\right) \quad (3)$$

in which PEoverall, PELDO and PECP are total, LDOs and charge pump PE.

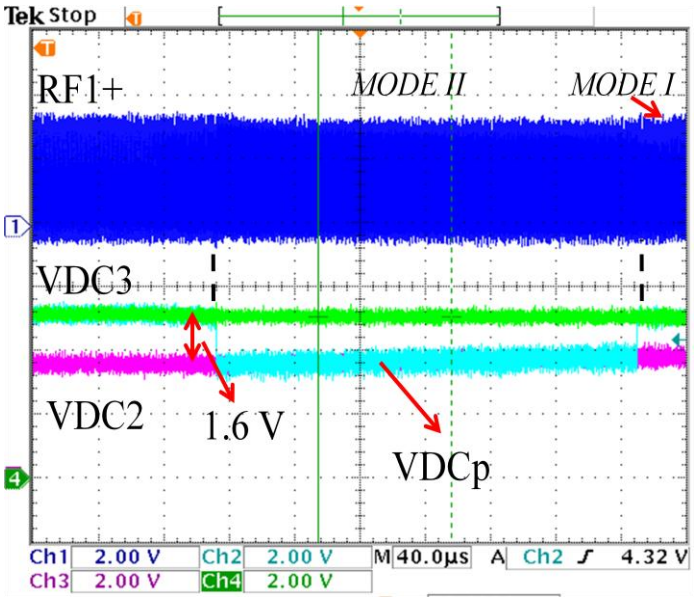
3.3.1 Rectifier Measurement

Fig. 3.14(a) shows the measured waveforms of the resonator tank output and the rectifier inputs. Operation mode I or II is determined by voltage of *VDC2* that should be maintained at an average voltage of 3.7V (3.6~3.8V). If it is less than 3.6 V, the rectifier is switched to mode II. If it is higher than 3.8 V, the rectifier is switched to mode I. In mode I, *RF1+* and *RS-* have same waveform (out of phase) and same amplitudes. In mode II, *RF1+* maintains its shape since its connection doesn't change from mode I. However, *RS-* amplitude decreases due to different loadings. Fig. 3.14(b) shows *RF1+* and the two outputs waveforms of the 2nd stage rectifier. It can be clearly seen that *VDC2* is being charged up in mode II.

Fig. 3.15 shows the measured power saving in the proposed 2-stage rectifier as compared to the conventional rectifier. The conventional rectifier is formed by simply connecting VDC2 to *VDC3* off-chip. Since *VDC2*/*VDC3*



(a)



(b)

Figure 3.14. Measured waveforms at inputs and outputs of the proposed 2-stage rectifier in different modes: (a) inputs to the rectifier and (b) input (*RF1+*) and outputs (*VDC2* and *VDC3*) of the rectifier.

voltage now needs to reach at least 4.2V for the charge pump, more DC power is consumed on *VDC2* in the conventional rectifier. The conventional rectifier shows higher wireless power transmission efficiency. However, the proposed rectifier still shows better system overall PE with maximum 4% improvement. In measurement, the load currents are 360µA/800µA for *VDC1*/*VDC3*,

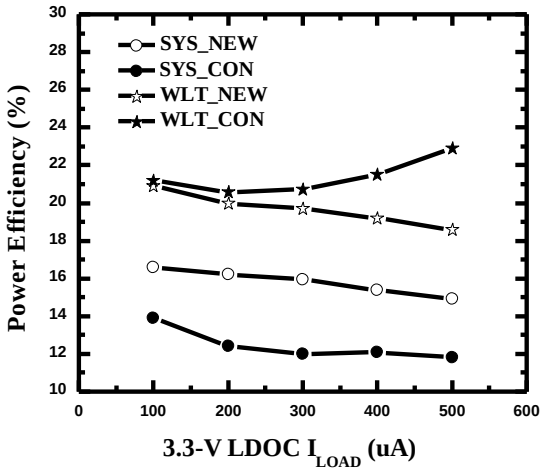


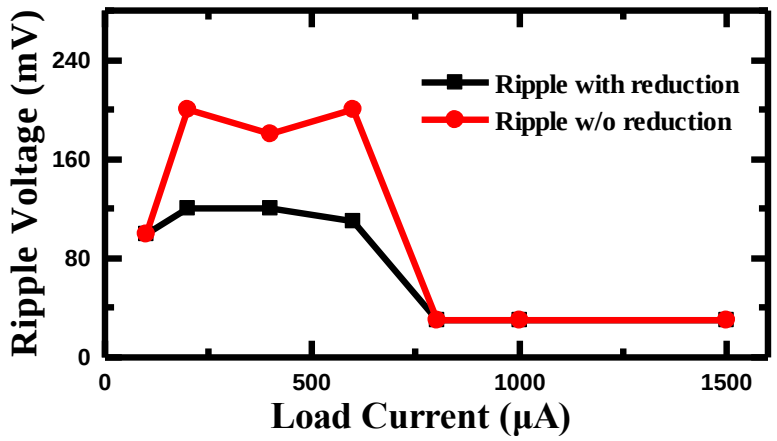
Figure 3.15. Measurement results of the proposed rectifier: *SYS_NEW* and *SYS_CON* are the overall power efficiencies, from signal generator to the output of the proposed and the conventional rectifier, respectively. *WLT_NEW* and *WLT_CON* are the wireless power transmission efficiencies, from signal generator to secondary coil, for the proposed rectifier and the conventional rectifier respectively.

respectively. Whereas the load current for *VDC2* is changed from 100 μA to 500 μA.

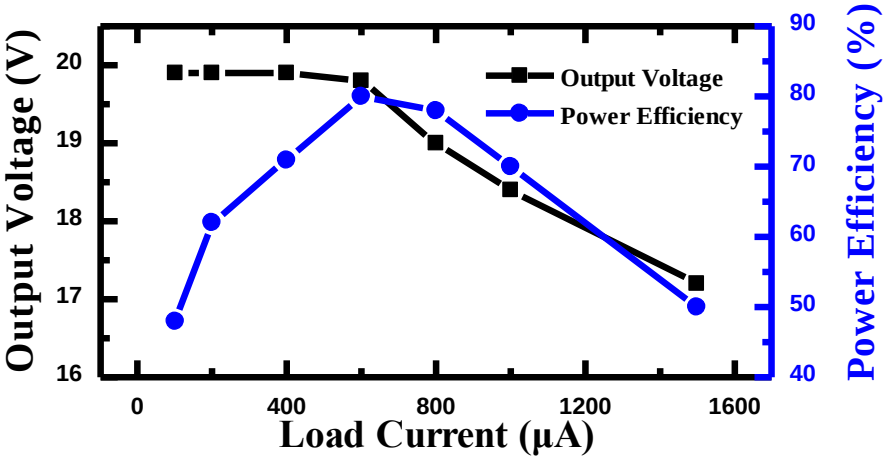
The conventional rectifier is formed by simply connecting VDC2 to *VDC3* off-chip. Since *VDC2*/*VDC3* voltage now needs to reach at least 4.2V for the charge pump, more DC power is consumed on *VDC2* in the conventional rectifier. The saved power on *VDC2* in the proposed rectifier is about 6.5% when *VDC2*/*VDC3* is 4.8V. Whereas AC power saving is 15%, including the extra DC clamp circuit at *VDC2* in the proposed rectifier. In measurement, the load currents are 120μA/200μA/80μA for 1.8V/3.3V/20V, respectively.

3.3.2 Charge Pump Ripple Voltage Reduction

Fig. 3.16 shows the measurement results of the charge pump with and without high-frequency clock for ripple reduction. It can be clearly seen that with the high-frequency clock, the ripples voltage is significantly reduced. As shown in Fig. 3.17(a), the ripple reduction in the proposed 2-clocks charge pump is around 40% when the load current is below 600μA. When the load current further increases, the DC output becomes lower than 20V (Fig.



(a)



(b)

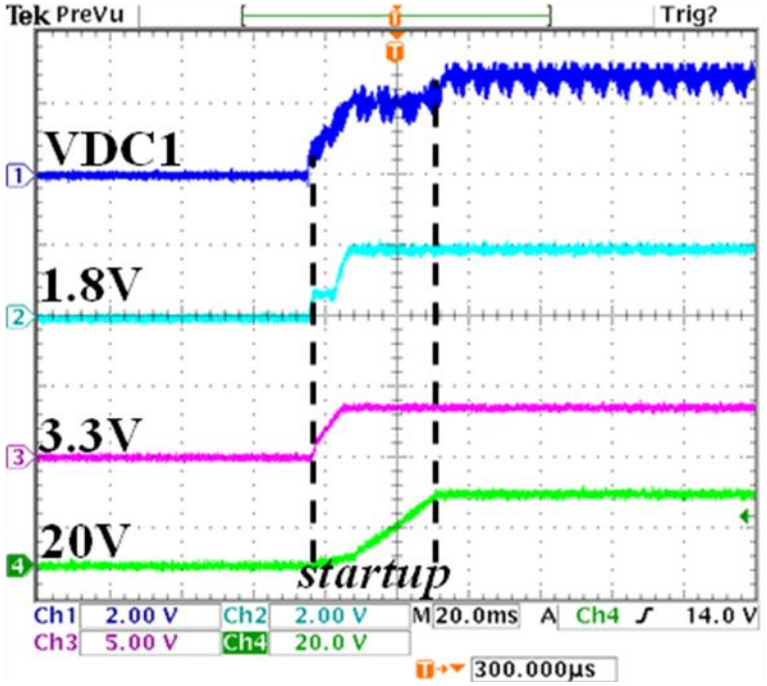
Figure 3.17. Measurement results of (a) charge pump output ripple and (b) the power efficiency vs load current.

3.17(b)), *CLKL* increases by the PFM control (> 1MHz) and thus the ripple is low and shows no difference between the two cases. As shown in Fig. 3.17(b), the charge pump achieves 82% peak efficiency at 600 μA load current. The output voltage can not be maintained at 20 V if load current further increases. The proposed 2-clocks scheme has no effect on the power efficiency.

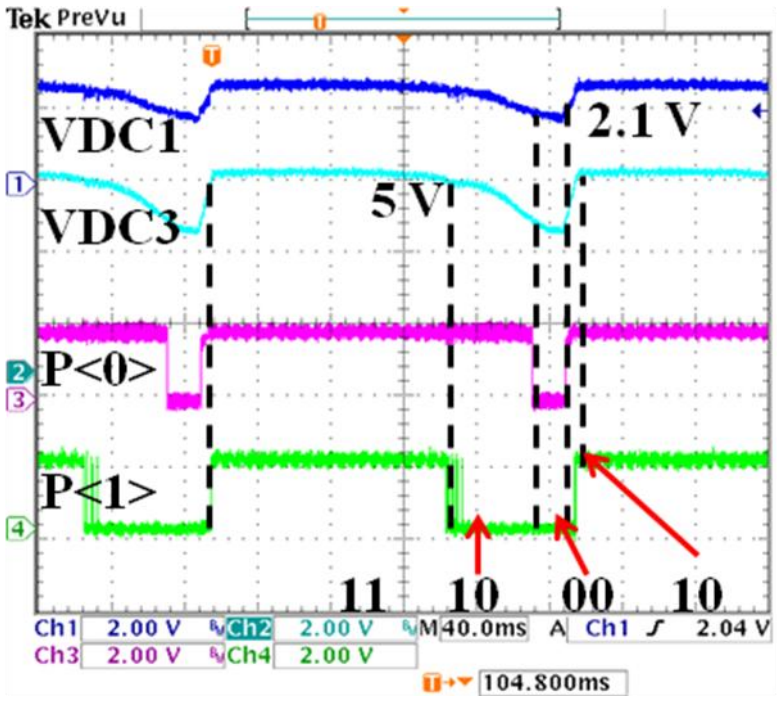
3.3.3 System Function Verification

Fig. 3.18 shows the startup sequence of the power management and power monitor function. Charge pump's start up is controlled by 1.8 V power-on-reset (POR) and *VDC3*. Hence, it is the last one to start working, as shown in Fig. 3.18(a). After the charge pump is started, *VDC1* reaches its highest value. This means that the charge pump absorbs large power during startup to charge the flying and load capacitors. Power monitor is measured when RF signal is modulated with low frequency to produce a varying RF power. Fig. 3.18(b) shows the power monitor states. When *VDC1* < 2.1 V, *p<0:1>* is "00", it means the received power is not enough or the circuit is starting up. When *VDC1* > 2.1 V, p<0:1> is "10", it means the received power is normal. When *VDC3* > 5 V, p<0:1> changes into "11", which means too much power is received and the clamp circuit is already activated. The closed-loop power control circuit should be activated to reduce the input power.

In forward data link measurement, a signal generator is used to generate power carrier with ASK modulation. Fig. 3.19(a) shows the forward data and clock recovery waveforms. The change of *VDCp* indicates that the rectifier changes from mode I to mode II and then back to mode I. *RF1+* is not influenced by the sudden rectifier mode change because of the unbalance



(a)



(b)

Figure 3.18. Measurement results of startup of the power unit and power monitor: (a) Waveforms of the power unit startup and (b) Waveforms of the power monitor measurement.

resonating. The signal on the carrier is successfully recovered by the CDR circuit. Fig. 3.19(b) is the zoomed-in view of Fig. 3.19(a), where it shows that

during the mode change, the ASK modulation on RF1+ is not affected. Fig. 3.19(c) shows that the 13.56-MHz clock is correctly recovered. In measurement, when *VDC3* voltage is below 5V, the rectifier mode transition cause <200 mV voltage change in *RF1+* envelope. But the CDR won't be affected as long as the voltage change is below 500 mV.

Fig. 3.19(d) shows the backward data link measurement. *DATA_in* is the data feed into LSK modulator and *DATA_rec* is the data recovered by the external data reader. Power monitor's status change is detected and transferred

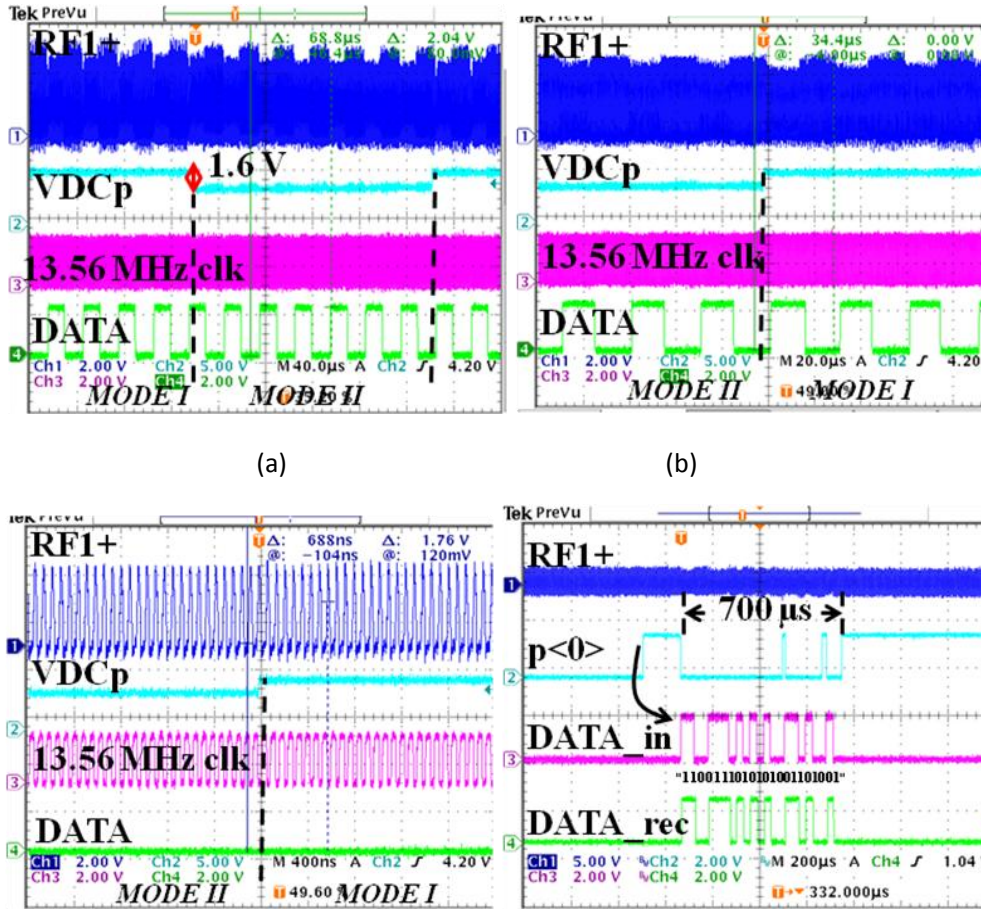


Figure 3.19. Measurement results of the bidirectional data link: (a) forward data link, *DATA* is the data recovered by CDR. (b) is the zoomed-in view of (a) and (c) is the further zoomed-in view of (b). (d) is backward data link.

to the external module in a data packet (*DATA_in*) through LSK modulator. The bottom trace shows the same data recovered by an external reader circuit. When LSK modulator is active, it will drain some current from the secondary coil. This temporarily causes the voltage to drop and *p<0>* changes to "0". This status won't be captured since the data sampling frequency is 1 kHz whereas the "0" duration is only 700 μs, and the next sampling is another 300μs later. After data transmission is completed, *p<0>* goes back to "1" again.

Fig. 3.20 shows measurement of the closed-loop power control function. *POW_contr* controls supply voltage of external class-E amplifier. *DATA_in* and *DATA_rec* are the data fed into LSK modulator and the data recovered by an external data reader. *POW_contr* is a 1-bit signal that controls the supply voltage of the class-E power amplifier to regulate the power transfer. Initially, *VDC3* exceeds 5 V, *p<0:1>* turns into "11". This information is transferred backward to the external module through coupling coils. The power control is

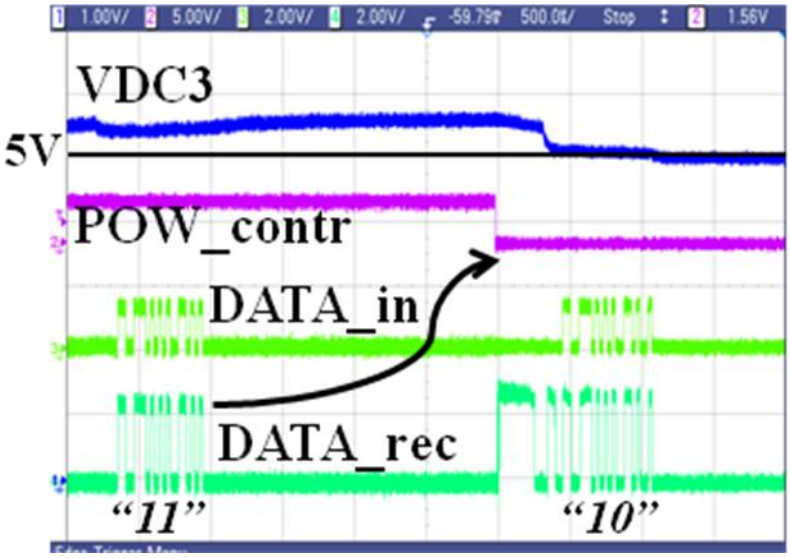


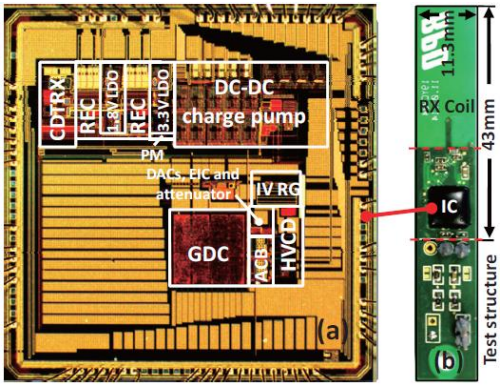
Figure 3.20. Measurement results of the closed-loop power control.

done through FPGA, which decodes the *DATA_rec* and turns *POW_contr* from high to low. The supply voltage of the class-E amplifier then decreases and reduces the power transferred to the secondary coil. Hence *VDC3* starts decreasing until *p<0:1>* becomes "10", which is represented by the second data of *DATA_in* in Fig. 3.20. This new data is fed back to the external module again, completing the closed-loop power control.

Fig. 3.21 shows a stimulator die photo with the proposed power/data recovery module. The integrated chip achieves 20V compliance voltage and maximum 1.24mA stimulation current. Fig. 3.21(b) shows a prototype implantable stimulator device consisting of the proposed stimulator chip, RX coil and off-chip components. The implantable device has been tested in lab environment.

3.3.4 Further discussion

The coils' distance would influence maximum power point transferring. Fig. 3.22 shows simulation results of received power at different coils' distances. Let coils distance be 5 mm. And suppose the equivalent load is point C, when



(a) (b)

Figure 3.21. (a) A stimulator die photo with the proposed power/data recovery module and (b) the implantable stimulator device

rectifier is in mode I. When rectifier is in mode II, equivalent load is lower, suppose it is point A. As the rectifier works, the final equivalent load is between point A and point C, likes point B. Point B shift between A and C, according to time ratio of mode I and mode II. When coils' distance changes, the received power varies, but still shows similar curve shape.

Fig. 3.23 shows the HV charge pump in different frequencies, at 10 kHz and 20 kHz. The charge pump output at 20 kHz is larger than the output with 20 kHz clock. However, the charge pump has a higher peak PE at 10 kHz clock. This HV charge pump is used in high output voltage, low load current application. 4 stages structure is adopted in charge pump design. Normally, charge pumps PE locate in 80% ~ 90%. But when 4 stages charge pump are series connected to provide HV output, PE becomes 66% (0.9^4). In this design, much low frequency clock and large flying capacitance are used to ultimately achieve 80% peak PE. Because higher frequency means smaller flying capacitance or larger power switches which deteriorates PE due to power

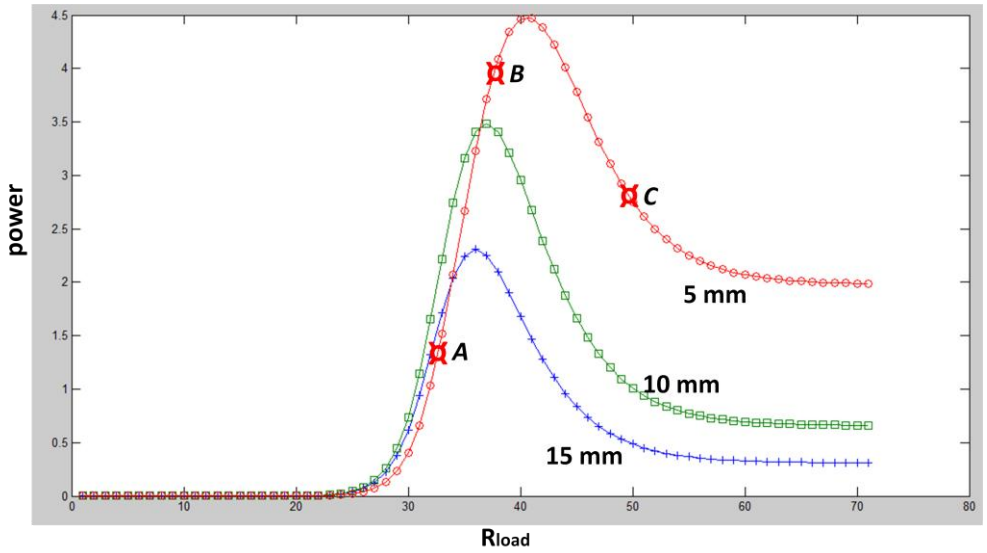


Figure 3.22. Received wireless power vs. equivalent load.

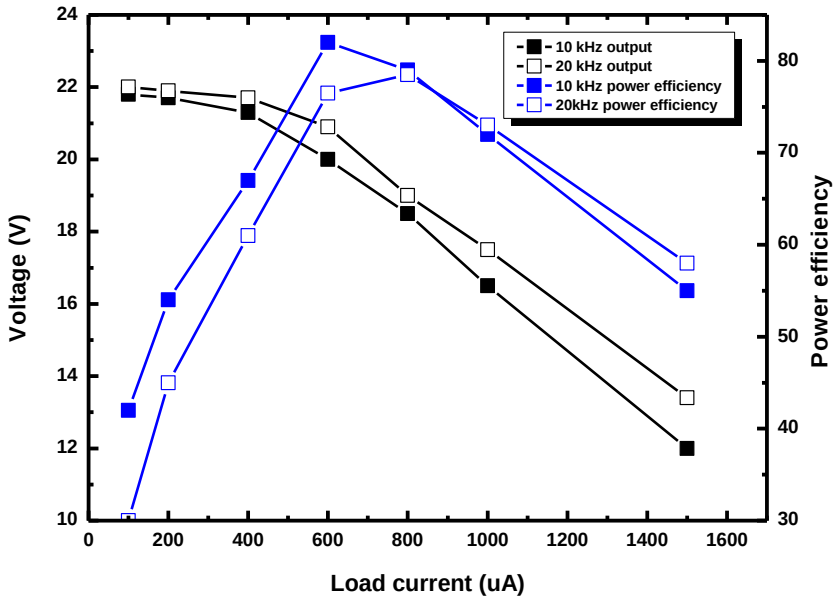


Figure 3.23. Received wireless power vs. equivalent load.

consumption on parasitic capacitors. Moreover, the charge pump takes 1/2 chip area in this power/data module, higher clock frequency demands much larger power transistors (with same W/L, HV transistors takes 10 ~ 20 times larger area than LV transistors for latch-up protection) which leads over large chip area for charge pump.

CHAPTER 4 A HIGH EFFICIENCY ACTIVE RECTIFIER EMPLOYING DUAL COMPARATORS WITH DIGITALLY TUNABLE OFFSET FOR CONDUCTION TIME OPTIMIZATION

This chapter proposes a technique that dynamically compensates the variable circuit delay and comparator offsets to prevent the reverse current. This technique also allows the rectifier to achieve high PE in a wide carrier frequency range and under varying input amplitude. The proposed technique is demonstrated in a fabricated chip for proof-of-concept. In this Chapter, the proposed rectifier and circuit implementation, as well as the measurement results will be presented.

4.1 The Proposed Rectifier with Dynamic Conduction Time Error Compensation

4.1.1 Operating Principle of the Proposed Rectifier

In order to achieve high power efficiency in varying carrier situation, tunable offset voltage comparator is proposed to compensate the conduction time error due to varying circuit delay and comparator offset. As shown in Fig. 4.1(a), the common-gate input comparator has two input transistors, M3 and M4. M4 is formed by an array of the transistors. By connecting different number of transistors to form M4, input offset of the comparator can be tuned.

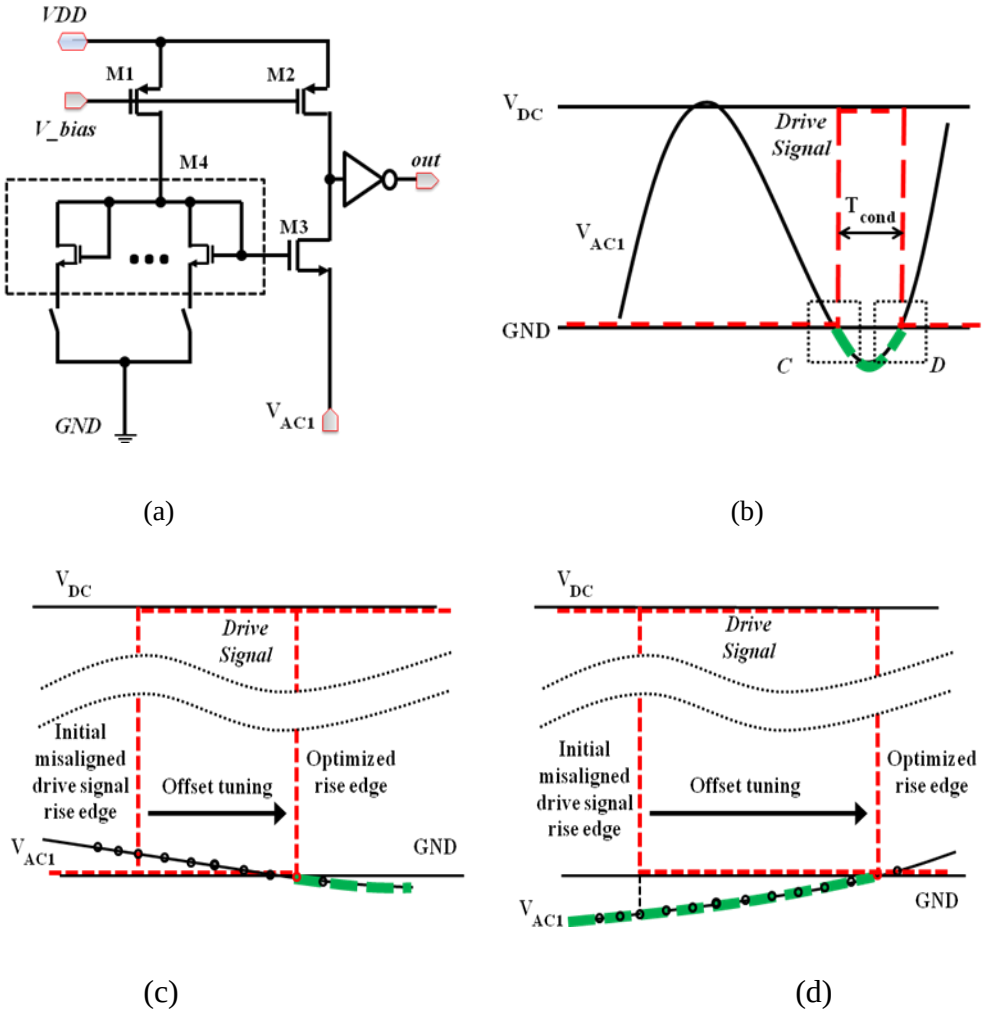


Figure 4.1. Illustration of tuning the conduction time by adjusting the comparator offset. (a) Offset tunable comparator. (b) Conduction time tuning. (c) Zoom-in view of rise edge tuning. And (d) zoom-in view of fall edge tuning.

A multi-bit offset tuning signal generated from the tuning logic circuit is used to tune the comparator offset. By setting the offset voltage at proper value, the correct drive signal (as shown Fig. 4.1(b)) that turns on/off conduct transistor with maximum conduct time without reverse current can be generated. Fig. 4.1(c) and Fig. 4.1(d) show the detailed conduction time correction process through the tuning of comparator offset. In Fig. 4.1(c), it assumes that there is an initial misalignment of conduction time (transistor is turned on (rise edge)

at a wrong time), as indicated. Through the feedback loop, the offset of comparator, CMP_R1, is tuned, so does the turn-on time of the transistor, until the conduction time is aligned correctly. Similar correction process applies to the turn-off signal (fall edge), as shown in Fig. 4.1(d).

To automatically monitor and correct the conduction time error, a feedback control loop is proposed. The AC signal is sampled/hold at the rise/fall edge of the drive signal, respectively. A polarity comparator compares the sampled value with "GND" to determine whether reverse current has occurred (When sampled value higher than "GND", revere current is induced and vice versa). Based on the polarity, offset tuning signal is generated to adjust the comparator offset until the optimum position is reached, as in Fig. 4.1(b).

Furthermore, each comparator in the conventional active rectifier is replaced by two comparators, among which one controls the turn-on of the conduct transistor and the other controls turn-off. A drive signal generator uses the turn-on and turn-off information from the two comparators to generate final drive signal to drive the conduct transistor. Fig. 4.2 shows how the final drive signal is generated. The two edge signals in Fig. 4.2(a) and Fig. 4.2(c) are combined to form the final drive signal (Fig. 4.2(b)) for the conduct transistor. Using the proposed two-comparator technique, the multi-conduction problem can be completely eliminated.

To be able to fine tune the comparator offset and accurately control the conduction time, the offset tuning needs to have fine resolution. In this work, the rise edge and fall edge comparators are designed to have 20 and 24 tuning levels, respectively. In this rectifier, the digital logic control can compensate the edge comparators offset. The offset is actually determined by the polarity

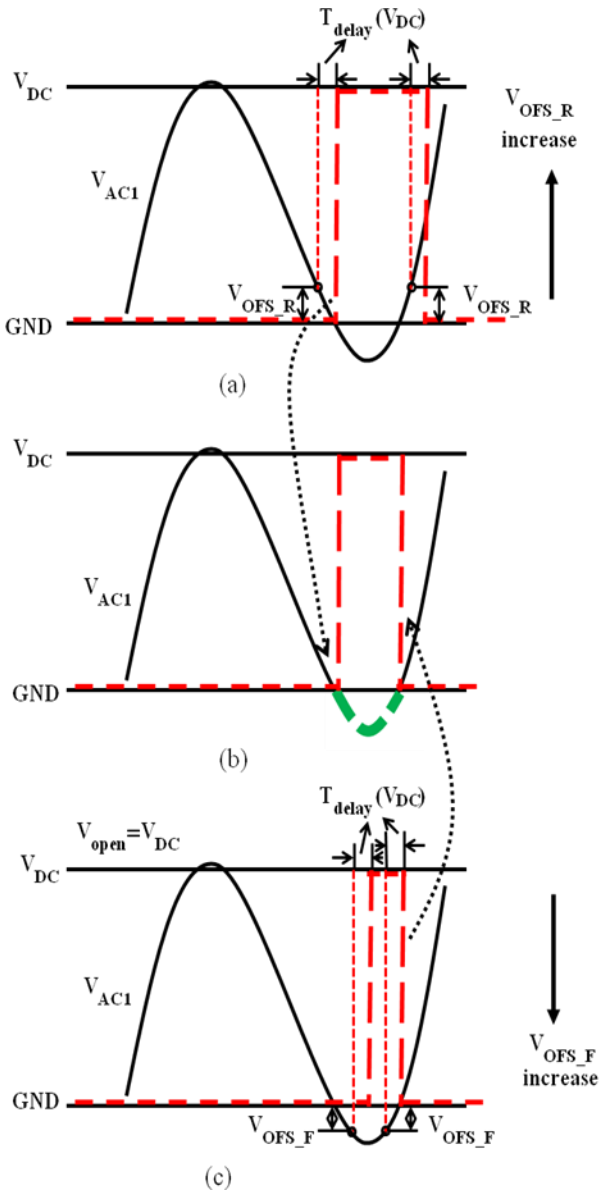


Figure 4.2. Illustration of two-comparator working principle (a) Correct rise edge control signal. (b) Final combined drive signal. (c) Correct fall edge control signal.

comparators. The polarity comparators input offset is designed to be around 5 mV and its offset can be changed by off-chip setting. In this design, the rise/fall edge comparators offset voltage tunable range is set to be 300 mV, divided by 20 and 24 levels. The tuning bits actually control offset voltage but not time delay since different amplitude or different frequency carriers mean different time delay. In simulation, less than 10 mV offset voltage influence

PE by 1~2 %. It should be noted that, when conduct transistor is turned on or off, the bonding wire equivalent series inductance causes oscillating noise on input, which may eventually set the tuning resolution. Thus, further increasing the tuning levels may not gain extra resolution.

4.1.2 The Proposed Rectifier Architecture

Fig. 4.3 shows the block diagram of the proposed rectifier. Two PMOS transistors M1 and M2 are cross-coupled connected, so the rectifier conduction is determined by M3 and M4. COM_R1 and COM_F2 are two common-gate input comparators whose offsets can be tuned in a wide range, and turns on (at rise edge) and off (at fall edge) M3, respectively. DRI_GEN1 is a custom-designed logic unit to combine COM_R1 rising edge and COM_F2 falling edge to generate drive signal for M3. S/H_Rise_Edge1 and S/H_Fall_Edge2 sample and hold V_{AC1} value at the moment when M3 turn on and off. COM_P1 and COM_P2 are two polarity comparators, which compare sampled V_{AC1} to the "GND" and output the polarity, that is, whether V_{AC1} is higher or lower than GND. The outputs of COM_P1 and COM_P2 are fed to T/L1 and T/L2 to generate the offset tuning signal for comparator CMP_R1 and CMP_F2. These circuits form a closed control loop to sense the conduction time error and dynamically correct it by tuning the input offset of the comparators (CMP_R1 and CMP_F2). The circuits on the right side that controls M4 is same as the circuit on the left. Apart from the sampling and holding circuit, the rest of the feedback loop circuits work at a frequency (clk_low_freq) lower than the carrier , shown as the dotted line blocks in Fig. 4.3. This reduces the overall power consumption. The conduction time

adjustment is also synchronized with this low frequency clock.

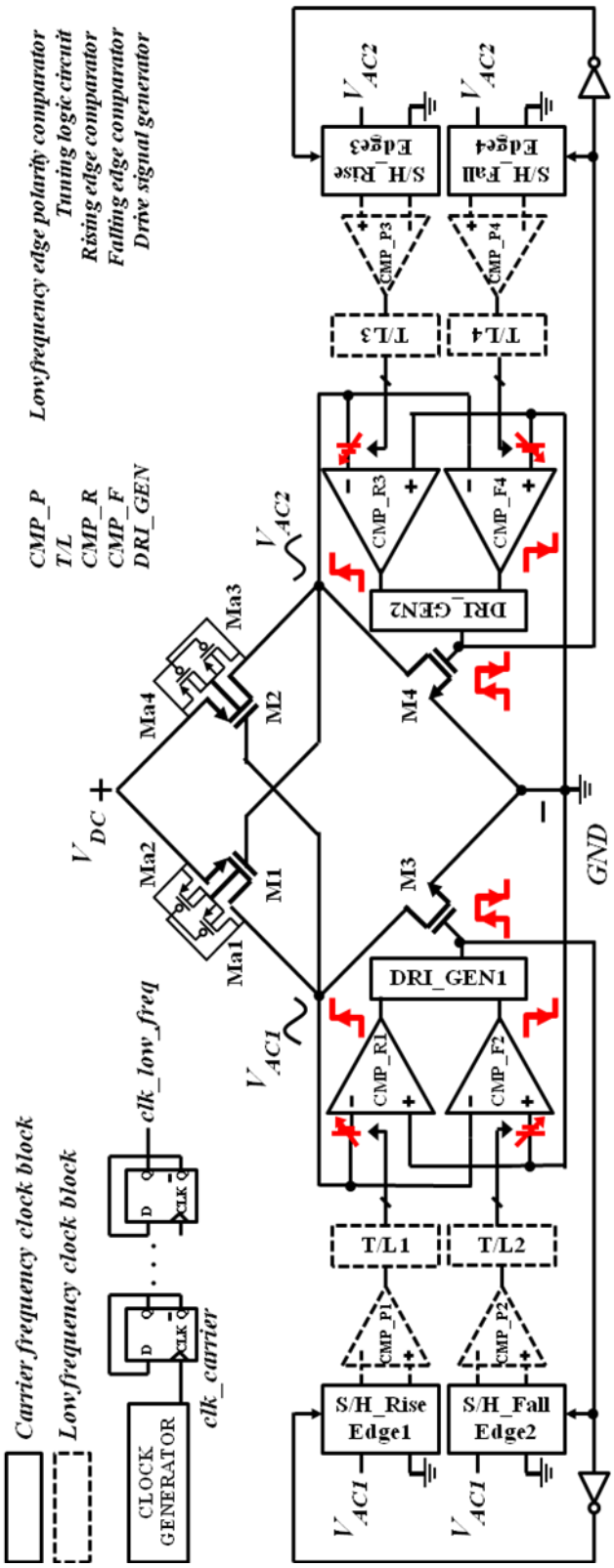


Figure 4.3. Block diagram of the rectifier in this paper.

Once the optimum conduction time is reached, the tuning logic will try to widen the conduct time without causing reverse current. This is because when the carrier frequency or amplitude changes, the conduction time may need to be adjusted to maximize the conduction. The widening is only performed in every 512 carrier clock cycles.

In this way, the tuning logic blocks are able to continuously track the optimum status of the rectifier, in case the carrier amplitude or load condition changes. At the same time, the tuning logic needs to prevent the reverse current. The reverse current is checked more frequently at clk_low_freq frequency (clk_carrier/32). More detail information about start-up will be presented in section 4.2.5, tuning logic circuit.

4.2 Circuit Implementation and Simulation Results

4.2.1 Clock Generator and S/H Circuit

Fig. 4.4(a) shows the schematic of the clock generator. Schmitt trigger inverter based clock recovery circuit converts the AC signal into a 50% duty cycle clock. A series of D-FLFPs down convert the clock recovered from the carrier to low frequency clock (clk_low_freq = clk_carrier/32) for the tuning logic and polarity comparators. The clock, clk_low_freq, is further down converted (to clk_low_freq/16) for the for the conduct time widening circuit. The conduction widening circuit is activated in every 512 carrier clock cycles.

Fig. 4.4(b) shows the schematic of the S/H circuit, S/H_Fall_Edge2. The sampling clock *clk1* is same with conduct transistor driver signal. *Clk2* is the complementary and non-overlap signal of *clk1*. When *clk1* turns to “low”, the sampled signal is the V_{AC1} as the conduct transistor turns off. The sampled

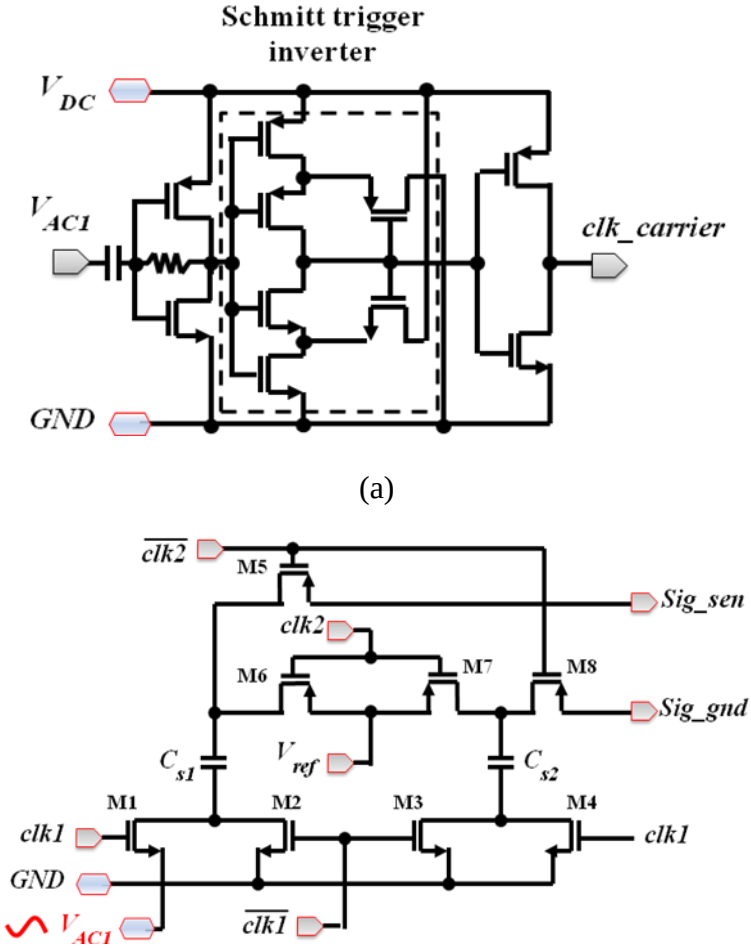


Figure 4.4. Schematic of (a) clock generator and (b) voltage Sampling/Holding circuit.

value is fed to polarity comparator in "high" phase of *clk2* and is compared with "GND". If sampled V_{AC1} is higher than "GND", reverse current occurs. S/H_Rise_Edge2 has the same schematic with S/H_Fall_Edge2, but it samples V_{AC1} as the conduct transistor turns on (when clk1 becomes "high").

Even though the S/H circuit operates at the clock frequency same as the carrier, the feedback loop polarity comparator after the S/H circuit use the low frequency clock, *clk_low_freq*, to reduce the power consumption without the performance deterioration.

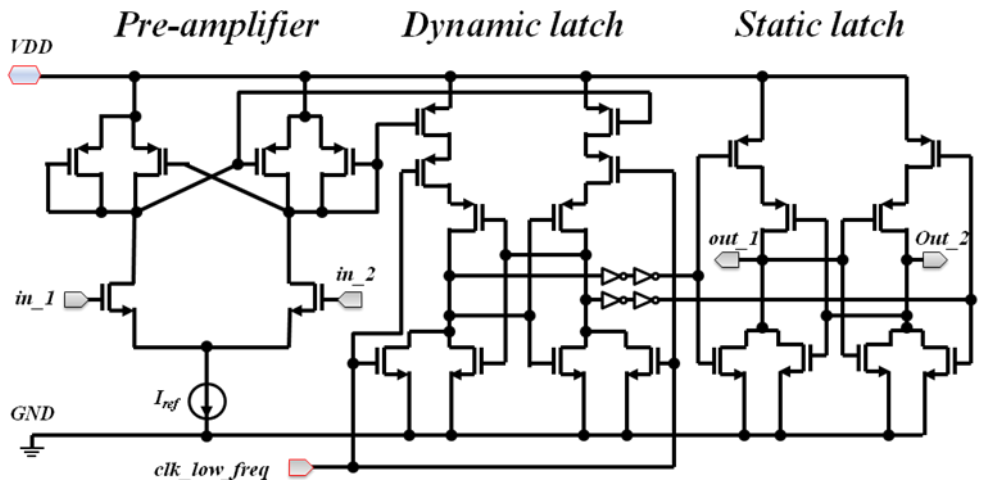


Figure 4.5. Schematic of the low frequency edge polarity comparator.

4.2.2 Low Frequency Polarity Comparator

Fig. 4.5 shows schematic of the low frequency polarity comparator. It consists of a pre-amplifier, a dynamic latch and a static latch. A regenerate amplifier is utilized to pre-amplify the voltage difference between V_{AC} and "*GND*" from S/H circuit. The cross-coupled NMOS transistor pairs in dynamic/static latch push the amplified signal into full swing digital signal. Buffers are inserted between the dynamic latch and the static latch to block the kickback noise from the static latch.

4.2.3 Offset Tunable Rise/Fall Edge Comparator

Fig. 4.6 shows the schematic of the offset tunable rise-edge comparator that generates the turn-on signal. Transistors M_{24} to M_{43} serve as switches which are digitally controlled to turn in or out the transistors from M_4 to M_{23} to form one input transistor, together with M_{44} act as the common-gate input stage. The tunable input transistor (M_4 to M_{23}) the aspect ratio of the transistors are designed from 0.4μm/6μm to 10μm/0.35μm, resulting in a linear offset change.

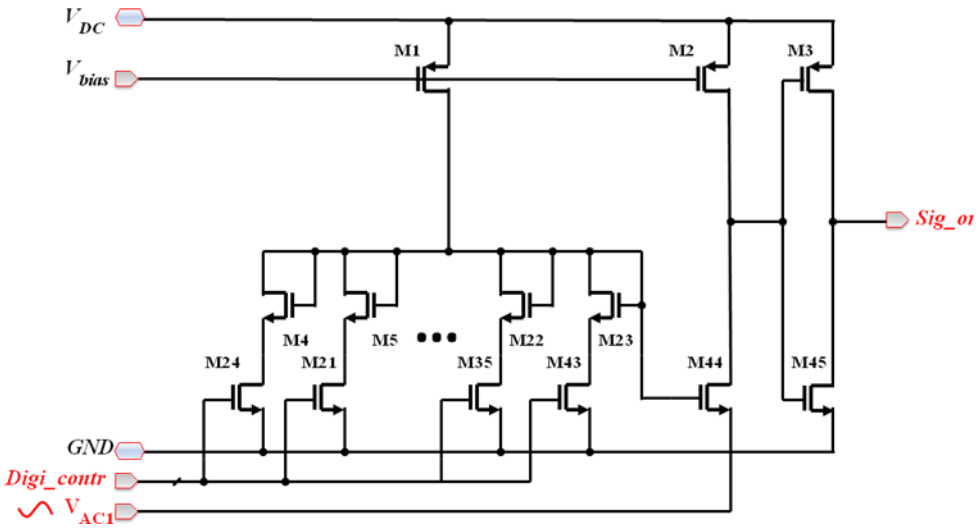


Figure 4.6. Schematic of the rising edge comparator.

If all the transistors are enabled, the total equivalent W/L of M4 to M23 is slightly larger than the aspect ratio of M_{44} (aspect ratio of M_{44} is 12μm/0.35μm).

The offset tunable fall-edge comparator is very similar to the rise-edge comparator except the pin "AC" and "GND" connections are interchanged with each other. Note that the fall-edge comparator demands much higher speed than the rise-edge comparator since the comparator has to turn to "1" and back to "0" in the period when V_{AC1} is smaller than "*GND*", as in Fig. 4.2(c). Thus, the fall-edge comparator consumes more power and needs more tuning levels (24 levels) to get similar resolution as the rise-edge comparator.

4.2.4 Drive Signal Generator

Drive signal generator is a custom-designed logic circuit to generate the final drive signal and control the conduct transistors. Fig. 4.7 shows the schematic and timing diagram of the internal signals from the drive signal generator. Usually, "1" duty of *Fall_edge* is narrower than "1" duty of the

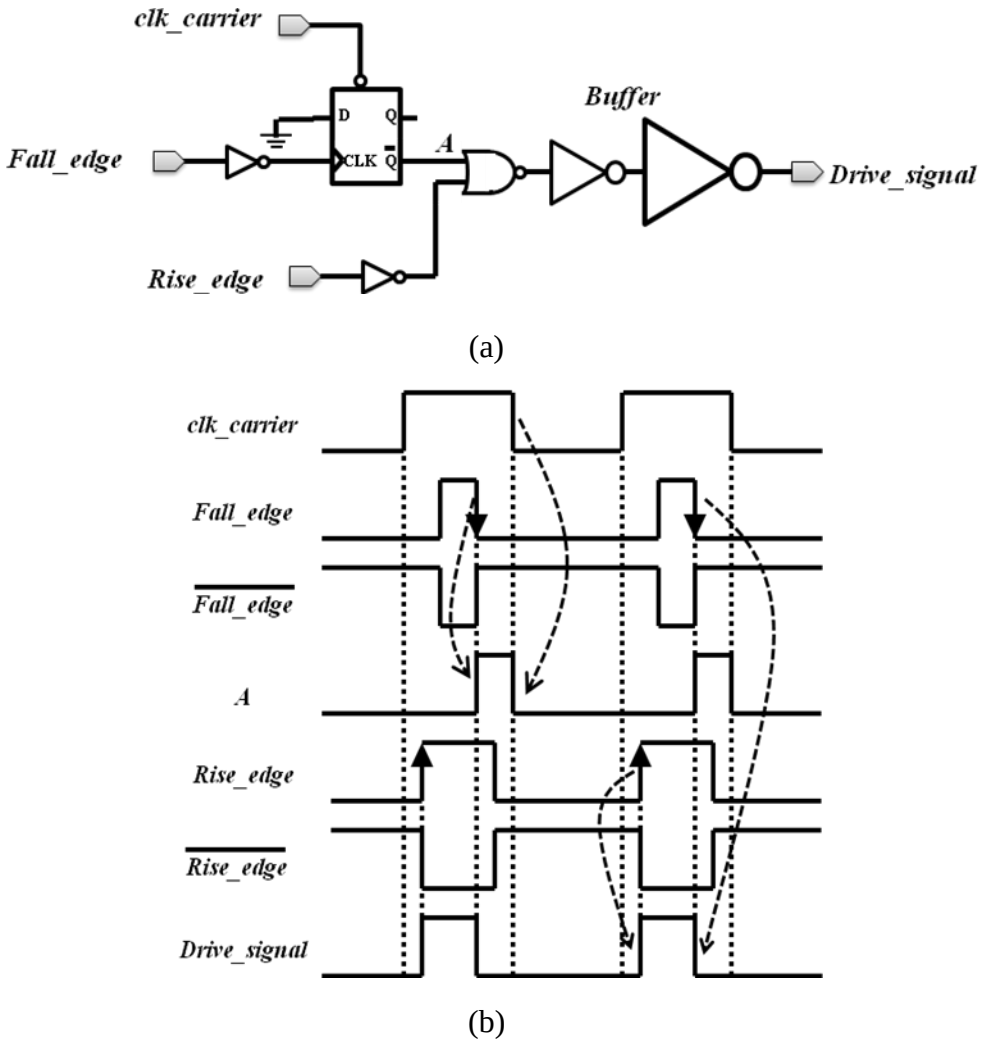


Figure 4.7. (a) Schematic of the drive signal generator. (b) Time sequence of the generator internal signals.

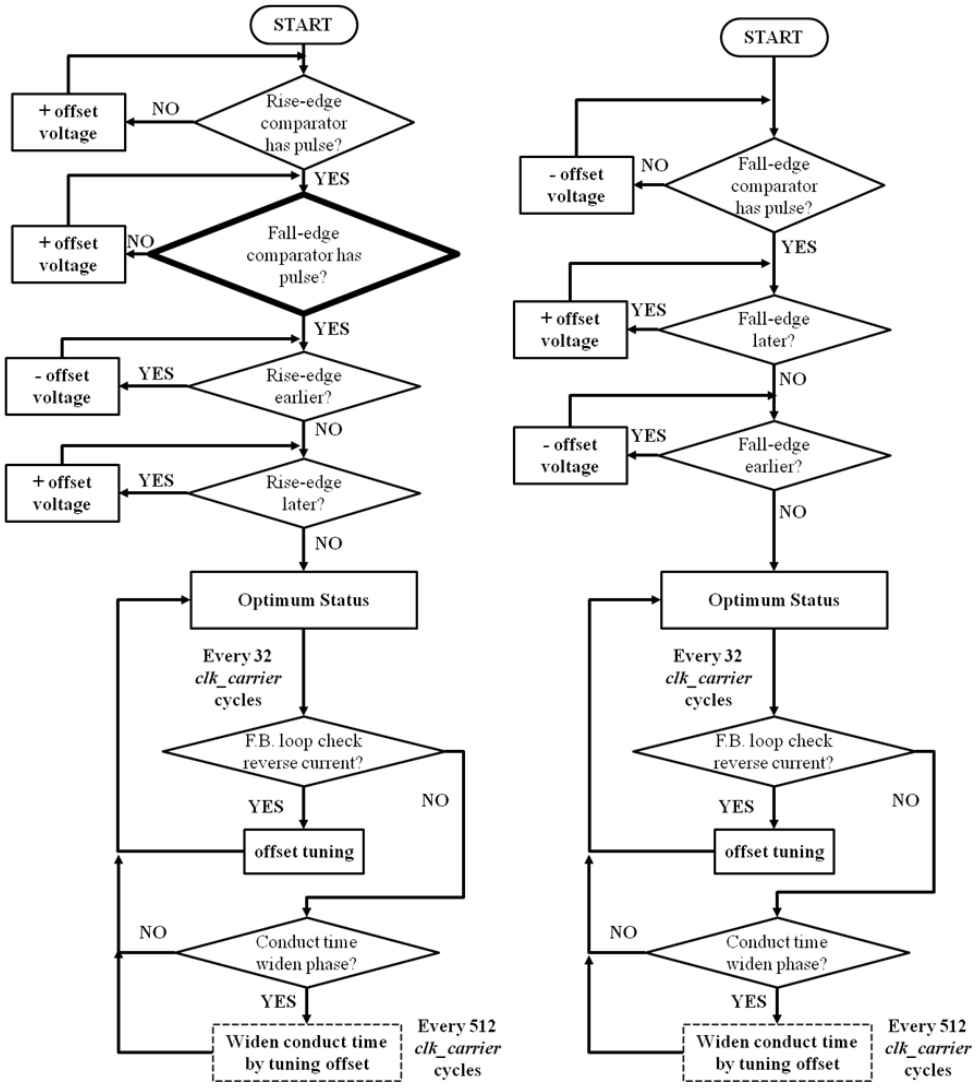
Rise_edge signal. The drive signal is generated by combining *A* and complementary signal of *Rise_edge* through a NOR gate. In this way, the effective rise and fall edges are combined together.

4.2.5 Tuning Logic Circuit

Tuning logic circuits (T/L1-T/L4 in Fig. 4.3) play a very important role in the proposed rectifier. In order to make the rectifier reliable, the tuning logic is designed to detect any possible abnormal status and adjust the rectifier back into normal working condition. Fig. 4.8 shows the flow chart of tuning logic

for rise-edge comparator and falling edge comparator, respectively.

When the rectifier starts up, if there are transitions (rise or fall) from the output of the rise-edge and fall-edge comparators, the tuning logic blocks will tune the offset voltages of these edge comparators such that the optimum conduction time can be achieved. Once the optimum conduction time is reached, the tuning logic will try to widen the conduct time without causing



(a) (b)

Figure 4.8. Flow charts of the tuning logic unit for edge comparators. (a) Flow chart of the rising edge comparator tuning logic. (b) Flow chart of the falling edge comparator tuning logic.

reverse current. This is because when the carrier frequency or amplitude changes, the conduction time may need to be adjusted to maximize the conduction, as described in Section 4.1.2. The widening is only performed in every 512 carrier clock cycles.

Another scenario is that there could be no rise/fall edge signals at all when the rectifier starts up since the carrier frequency and voltage amplitude are uncertain or have not been stabilized. The tuning logic would treat searching fall edge signal as the first priority. Rise-edge comparator will increase its input offset voltage to guarantee that it has no influence on the fall edge signal during the search searching, as shown by bold line box in Fig. 4.8(a). The fall-edge comparator will decrease its offset voltage simultaneously. After the falling edge signal appear, the offset tuning logic will search optimum working status by continually tuning offset of comparators. Noted that, offset voltages of the two comparators have opposite polarity (V_{OFS_R}>"GND", V_{OFS_F} <"GND") and their increasing directions are indicated in Fig. 4.2.

4.2.6 Simulation of the Rectifier

Fig. 4.9 shows the simulation waveforms of the rectifier. When rectifier starts up, the initial offset voltage of the comparator is set externally. After stable V_{DC} is established for the circuits in rectifier, tuning logic starts working and automatically tune offset voltages of the edge comparators. The offset tuning status can be seen in Fig. 4.9. A 13.56 MHz, 2 V amplitude sine wave voltage source is used as a carrier in the simulation.

Fig. 4.10 shows the pie chart of the rectifier power consumption. The largest power consumption part is from the edge comparators since they need

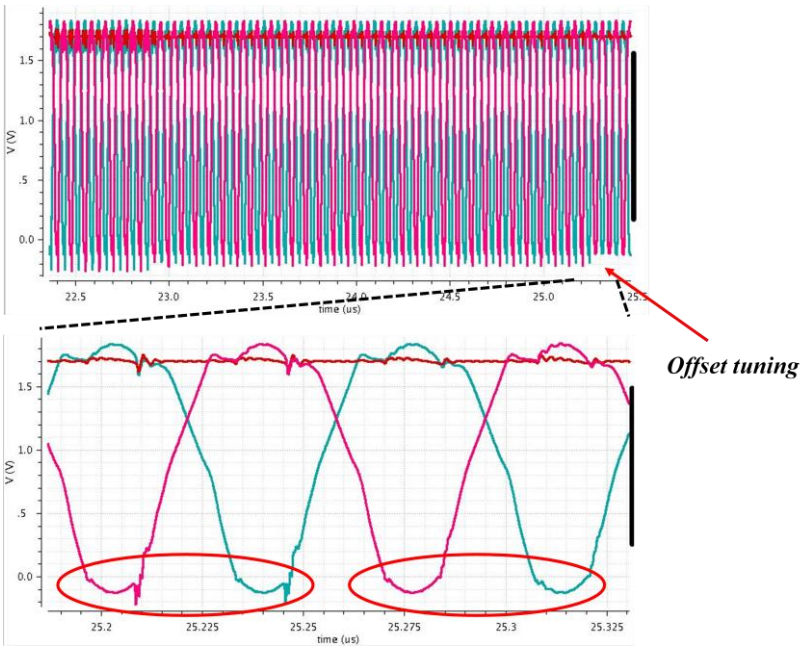


Figure 4.10. V_{AC} waveforms of the rectifier simulation.

to operate at high speed to for 13.56-MHz carrier. The other circuits, including S/H, polarity comparators and digital edge combining circuit consume around 20% of the total power . The logic tuning blocks consume the least power as they operate at low frequency. The total simulated supply current is 210 μA at 2 V DC output voltage with 13.56-MHz carrier. The simulation show that the

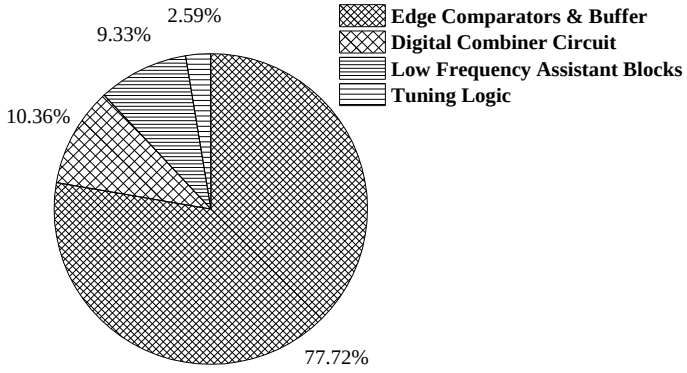


Figure 4.9. Pie chart of blocks power consumption in simulation.

rectifier functions well at 2V and 13.56-MHz carrier.

4.3 Measurement Results and Discussion

The rectifier was fabricated in a 0.35-μm CMOS technology and occupied a 0.3 mm^2 active area. Fig. 4.11 shows the chip microphotograph. In measurement, an Agilent 33250A signal generator is used to drive the rectifier. The load resistor is set manually on PCB, and the load capacitor is 1μF in all measurements. In PE measurement, a 10 Ω series connected resistor is inserted between signal generator and the chip to measure the input current.

Fig. 4.12 shows the measurement waveforms with two carrier frequencies. The rectifier works well in the carrier frequency range from 100 kHz to 13.56 MHz. However, it works more stably in lower frequencies than in higher carrier frequencies. This is because the equivalent series inductance in package and bonding wire introduces oscillating noise which may affect the comparator performance in higher carrier frequency.

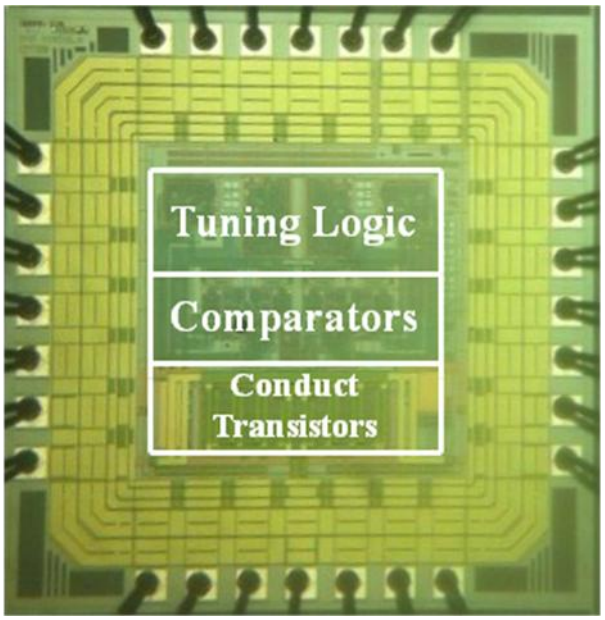
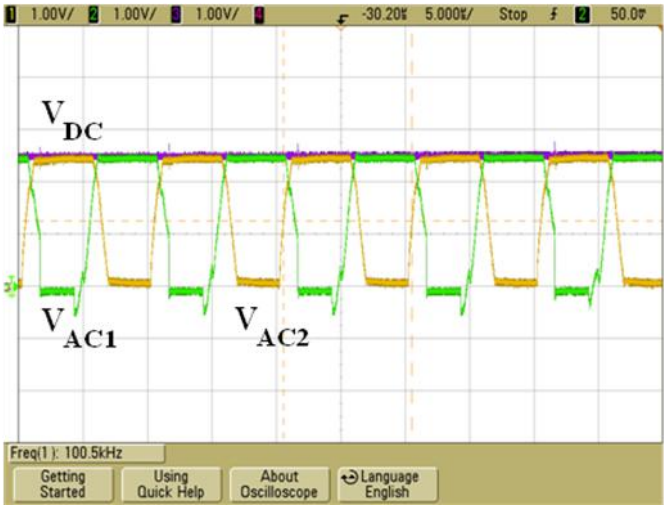
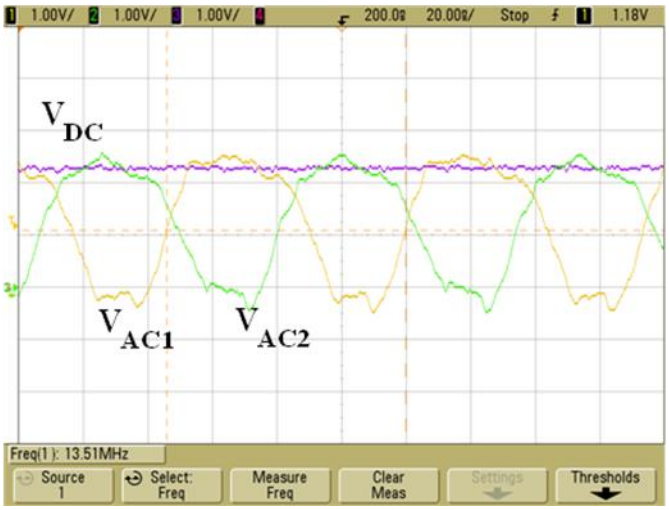


Figure 4.11. Die photo of the fabricated rectifier.



(a)



(b)

Figure 4.12. Measurement waveforms of the rectifier. (a) Carrier frequency is 100 kHz. (b) Carrier frequency is 13.56 MHz.

Fig. 4.13(a) shows the rectifier PE versus carrier frequency and comparison with some previous works. The measurements are done with a 500-Ω load resistor and 1-μF capacitor under 2 V DC output voltage. The previous works only have PE reported at one frequency are not included. The rectifier in this work is able to operate in the widest input frequency range (100 kHz – 13.56 MHz). Generally, all the rectifiers show higher PE performance in lower frequency than in higher frequency, because the conduct transistors turn on

and off more frequently and thus cause high power consumption.

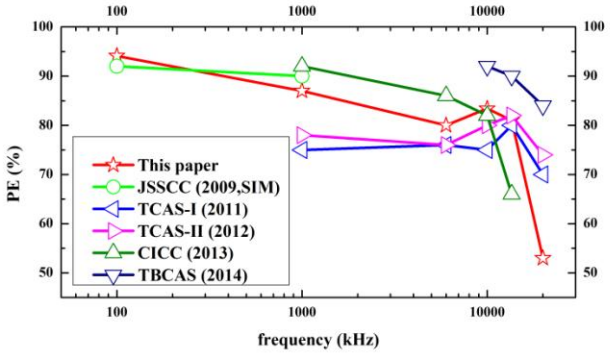
Fig. 4.13(b) shows the PE vs. the output DC voltages at 13.56 MHz. Except the design using dynamic biasing in [68], although the peak PEs of other designs are all above 80%, but in a small DC output voltage range. It should be noted that the rectifier in this work achieves larger than 80% PE not only in a wider carrier frequency range, but also in wide DC output range.

Fig. 4.13(c) shows the rectifier PE versus DC output voltage for different carrier frequencies. PE vs. V_{DC} curves are relative flat, thanks to the tuning algorithm of the rectifier. At higher carrier frequencies, PE drops as V_{DC} voltage increases because the rectifier is optimized at 2 V.

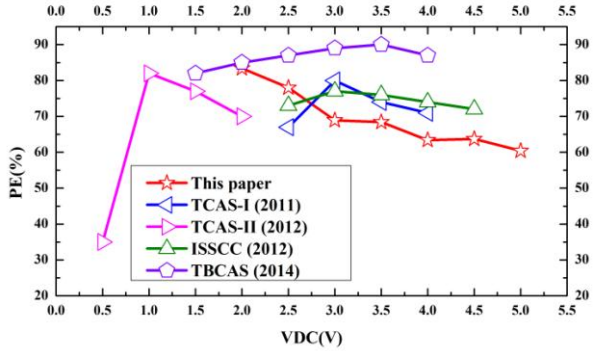
Fig. 4.13(d) shows the rectifier PE versus the resistive load. The PE achieves peak value at a certain point (the resistance is optimized to be 500 ohms) in higher frequency range. Because in higher frequency range, the peak conduct current is larger than in lower frequency with the same resistive load.

Several issues cause the rectifier's lower PE in higher carrier frequency. Firstly, edge comparators and drive signal buffers have higher power consumption in higher frequency. Secondly, bonding wire equivalent inductance and resistance generate larger noise, which affect the performances of both edge comparators and polarity comparators at higher carrier frequency, thus resulting in lower PE. Finally, the rectifier has some digital ancillary circuits to support the operation of the tuning logic block, which consumes more power at higher carrier frequency and V_{DC}, as they operate at carrier frequency.

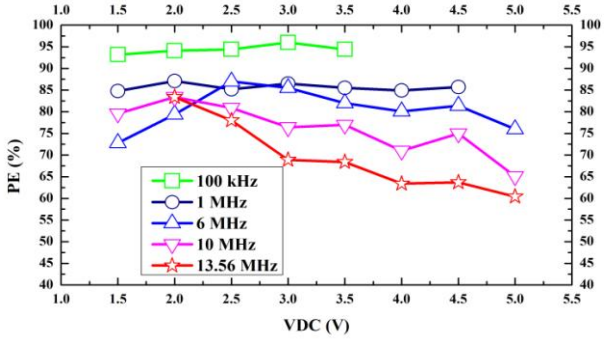
The performances of the rectifier in this work and the some previous works are summarized in table 4.1. The rectifier in this paper shows a high PE (≥



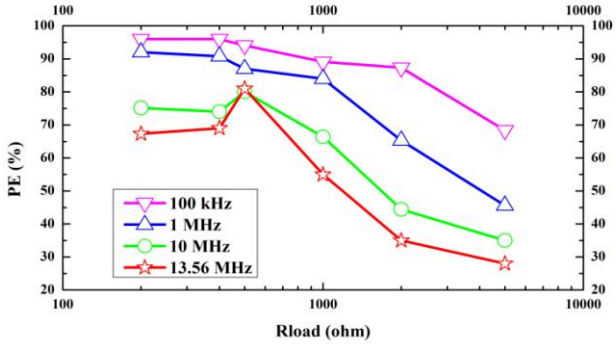
(a)



(b)



(c)



(d)

Figure 4.13. Measured rectifier PE performance and comparisions. (a) PE vs. carrier frequency. (b) PE vs. output V_{DC} at 13.56 MHz carrier. (c) PE vs. output V_{DC} for different carrier frequencies, (d) PE vs. rectifier resistive load R_{load}.

80%) in the wide DC output range at the carrier frequency ≤ 6MHz and the

Table 4.1 Rectifier characteristics comparison table

	JSSCC 2009[61]	TCAS-II 2012[62]	TCAS-I 2011[64]	ISSCC 2012[65]	CICC 2013[67]	TBCAS 2014[68]	This paper
Process	0.35µm CMOS	0.35µm CMOS	0.5µm CMOS	0.5µm CMOS	0.18µm CMOS	0.35µm CMOS	0.35µm CMOS
Area (mm^2)	0.4	0.009	0.18	0.58	0.07	0.186	0.3
Frequency (MHz)	0.2 - 1.5	13.56	13.56	13.56	1-10	10-13.56	100k-13.56M
VAC (V)	2.4	1.5	3.8	3.7	NA	1.5-4	2~5.5
VDC (V)	2.08	1.33	3.12	3.1	2-3	1.19-3.56	1.5-5
R_{load} (Ω)	100	1 k	500	500	500-1.25k	500-1.8k	500
PE (%)	87 (SIM)	81.9(PEAK)	80.2(PEAK)	77(p)	>80	82.2-90.1	>90@100kHz >85@1MHz 83.4(PEAK)@13.56MHz

widest carrier frequency range (from 100kHz to 13.56MHz) compared to the previously reported designs. It is well suited for the implantable biomedical systems with output power in milliwatts range.

CHAPTER 5

CONCLUSIONS AND FUTURE WORK

5.1 Conclusions

In the thesis, a power/data recovery system for high-compliance-voltage stimulation has been described, in which several techniques to improve power efficiency have been proposed. A full-wave active rectifier with wide carrier frequency range has also been proposed and demonstrated in CMOS technology.

The wireless power management and data telemetry IC for high-compliance-voltage electrical stimulation applications is demonstrated in a 0.18-μm CMOS technology. The chip is powered by 13.56MHz RF carrier and generates 1.8 V, 3.3 V and 20 V supplies. The proposed unbalance resonating L-C tank and the time-division 2-stage rectifier generate three supplies for two LDOs and the charge pump, respectively, to improve the power efficiency. In the 20V charge pump implementation, the 2-clocks technique is proposed and reduces the ripple voltage by 40 % without degrading the charge pump efficiency. Bidirectional data link is successfully verified in the measurement with data rate of 61.5 and 33.3 kbps respectively. Closed-loop power control is also verified based on the power monitor integrated in the chip. The power management and data telemetry module could be used for fully implantable HV compliance nerve/muscle stimulator.

The full-wave active rectifier with digitally controlled offset tuneable comparator has been presented. It is believe that this is the first time the digital

logic feedback control is introduced into the active rectifier design. It is previously only implemented in analog domain. The tuning logic controls the offset voltage of comparators to dynamically compensate the conduction time error caused by circuit delays and comparator offsets. Two-comparator topology is proposed to completely eliminate the multi-conduction phenomenon that exists in most previous works. The measurement results have shown that the rectifier achieves at least 80% PE in the DC output voltage range from 2 to 5 V with carrier frequency from 100 kHz to 6 MHz and under a 500 resistive load. At higher frequency range (6 MHz – 13.56 MHz) the rectifier has also achieved larger than 80% peak PE at DC output voltage of 2V. This rectifier is well suited for the implantable biomedical systems that require high-efficiency power management circuit.

5.2 Future Work

In the power/data recovery module design, the 20V output current load capability is 800μA. Which may be not enough for some applications . In the future version, the 20V charge pump could be further improved to supply much more current with relatively small chip area. In addition, the rectifier in the module is a passive rectifier for its reliability to verify the system function. A multi-stage active rectifier, shares the passive rectifier topology, could be employed to enhance the overall system PE.

In the wide frequency range active rectifier, to reduce chip area, some function blocks, such as tuning logic circuit and polarity comparators, could be reused by the two conduct transistors. This can be achieved by using faster and more complex clock and save two set of data for different sides in D-

FLFPs. To further improve PE performance at 13.56 MHz carrier, a raw/simple/low current consume regulator can be used to drive the digital combiner circuits to enhance PE at higher V_{DC}. Advanced technology may be used to improve PE as the speed of comparators and logic circuits can be improved at lower power consumption .

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